LSI Testing: A Core Technology to a Successful LSI Industry

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Abstract—Despite its ever-growing importance in all innovation fields, such as automotive and IoT applications, the LSI industry is fragile due to its a weak technology-business chain. In addition, its products, namely LSI chips, are vulnerable to six risks (defective chip escape, radiation, aging, malicious attack, counterfeiting). LSI testing is the technology that is indispensable to mitigate these risks. This paper highlights the intent of LSI testing as well as its impact on the LSI industry.

I. Introduction

LSI (Large Scale Integration) chips or LSIs are one of the most important inventions of mankind. Since its birth, ever-growing scaling, ever-increasing complexity, and ever-shrinking process feature sizes have made LSIs an indispensable part of the modern society and industry. Nowadays, LSIs have become the key to all major innovations, including AI (Artificial Intelligence), VR (Virtual Reality), big data, AD (Autonomous Driving), IoT (Internet of Things), and robotics.

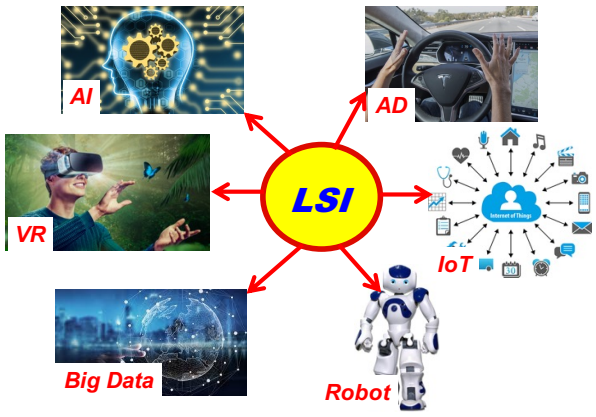


Fig. 1 LSI: The Key to All Innovations

Although being a strategic industry with unprecedented importance, the LSI industry is fragile due to the weakness in its technology-business chain. In addition, LSIs are subject to six major risks. In order to mitigate these risks, LSI testing has become an indispensable core technology to the LSI industry. In the rest of this paper, the intent and impact of LSI testing will be briefly described. The purpose is to highlight the importance of LSI testing.

II. Driving Forces for the LSI Industry

Fig. 2 shows the global LSI industry outlook from 2006 to 2021. It can be seen that the LSI industry is getting out of the slump caused by the COVID-19 pandemic and is returning to a very high growth rate.

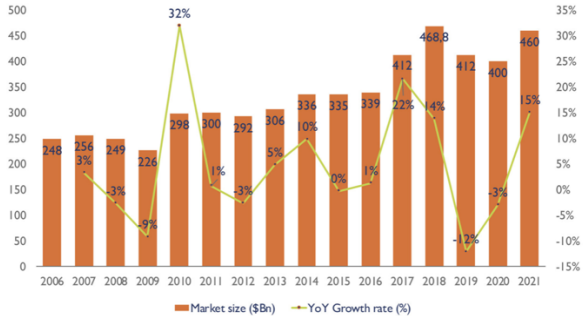


Fig. 2 Global LSI Industry Outlook

Fig. 3 shows the share distribution of 2017 LSI sales. Although standard PCs and cellphones consume most of LSI chips, automotive and IoT applications have top growth rates. This indicates that automotive and IoT devices will become the driving forces for the LSI industry.

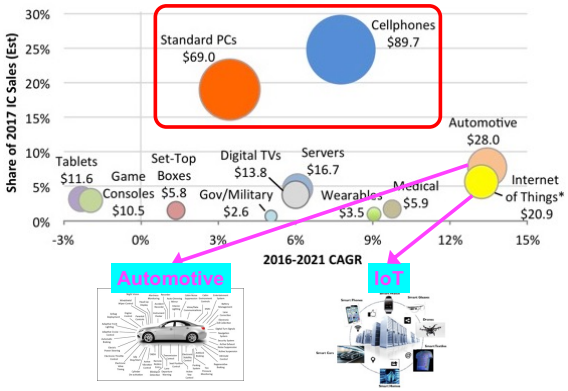


Fig. 3 Driving Forces for the LSI Industry

The major trend for cars is CASE (Connected, Automation, Sharing, Electrification). Expected benefits of CASE includes the ever-existing-and-growing market, the need for all types of LSIs, and the high entry barrier. Its potential challenges include high quality at low cost (0-defect w/o TMR), long-term reliability, and legal liability (level-3 AD and above). On the other hand, IoT devices usually need to achieve ultra-low-power (1mW) and have to employ emerging memory and edge AI. The potential problems of IoT devices are low selling prices, edge security concerns, and reliability worries in harsh environment.

III. LSI Technology-Business Chain

As illustrated in Fig. 4, the LSI technology-business chain consists of four major fields, namely design (including both functional design and design for test), manufacturing, packaging, and testing. The supporting sectors for the LSI industry include EDA (Electronic Design Automation), wafer, photoresist, photomask, and equipment companies. The producing sectors for the LSI industry include IDM (Integrated Device Manufacturer), fabless, foundry, packaging, and testing companies.

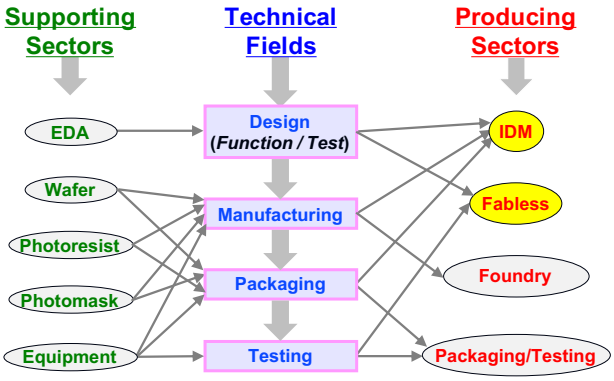


Fig. 4 Major Sectors in the LSI Industry

Despite the wide-recognized importance of the LSI industry, its technology chain is astonishingly fragile as illustrated in Fig. 5. Many of its sectors are monopolistic, in that one sector is often served by only one or two dominating suppliers. For example, the mask aligner sector is dominated by ASML, the MPU-IP sector is dominated by ARM, and the test EDA is dominated by Mentor Graphics. Therefore, these factors are highly vulnerable to disruptive risks. For example, SoftBank purchased ARM in 2016 and then sold it to Nvidia in 2020, Simens took over Mentor Graphics in 2017. Although those past transactions were friendly and smooth, there remain high risks that some future business maneuvers may get hostile and cause huge damages to customers. In addition, natural disasters, terrors, and wars can easily cause catastrophes to the LSI industry.

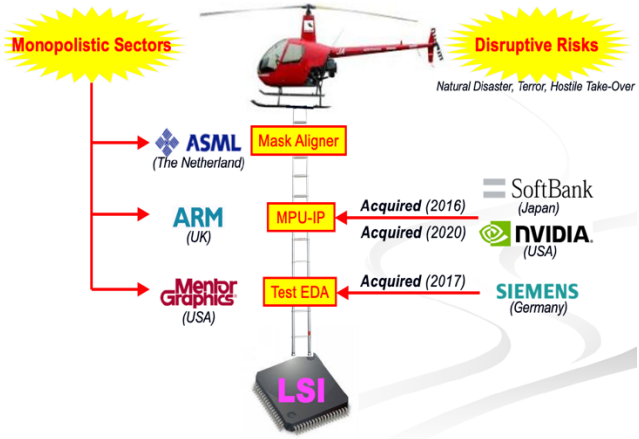


Fig. 5 LSI: A Fragile Industry

The LSI industry is so unique that business models and strategies commonly effective in other industries often do not apply. It is thus imperative that special attention be given to the unique properties of LSI: a fragile industry.

IV. Five Risks of LSIs

Despite of their significant importance and high impact, LSIs are nonetheless extremely vulnerable to six major risks as shown in Fig. 6. It is necessary to be fully aware of these risks and to take proactive measures to prevent them from causing severe harms to the producers and users of LSIs.

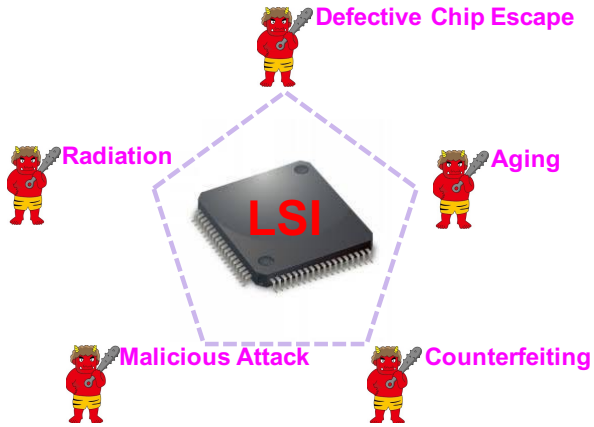


Fig. 6 Six Risks of LSIs

● ***Defective Chip Escape***: Defective LSIs may be shipped to the market and result in dire consequences. For example, a company made a 100M$ recall of HDDs due to defective LSIs (defect rate = 0.8%). Defective AI LSI chips may have poor accuracy. It has been reported that the inference accuracy is ideal if the yield of the RRAM used to implement a crossbar-array-based weight matrix is 97.8%. However, if the yield of RRAM drops to 95%, 90%, and 80%, inference accuracy will be reduced by 37%, 59%, and 69%, respectively. Such low accuracy will result in accidents if the AI LSI chips are used for autonomous driving.

● ***Radiation***: High-energy particles, such as Alpha particles from LSI packages, cosmic neutrons and protons, as well as thermal neutrons, may flip the states of FFs or SRAM cells in LSIs, causing transient LSI abnormality, called soft errors. It has been reported that soft errors shortened the orbit life of small satellites built with commercial LSIs and caused workstation failures at VeriSign (a US-based domain name registry service company), resulting in huge losses for many internet companies using its service.

● ***Aging***: LSI chips may fail due to field degradation, including physical and electric stress, dielectric breakdown, bias temperature instability. LSI defect rates generally grow in time and/or in harsh environment. The impact of LSI aging poses a severe risk for cars, airplanes, railway, infrastructure, etc. For example, a time-dependent dielectric breakdown in a single LSI chip used in an exchange system once caused phone service outage in central Tokyo, Japan.

● ***Malicious Attach***: Trojan circuitry may be inserted in an LSI during outsourced design and manufacturing. It can then be used in malicious attacks again the resulting LSIs. It has been reported that a Trojan block was found in an electric iron that could invade Wi-Fi-connected PCs in 200m around it. Trojan circuitry was also found in LSIs used in weapons, transportation, nuclear plants, etc. in the US. It is widely known that someone may steal secrets from a PC or smartphone through side-channel attack against encryption LSIs by analyzing power dissipation, fault information, and timing information. Generally, every system is risky if it uses LSIs and the internet. Cars are a typical example since they use many LSI-based ECUs (Electronic Control Units) and are connected to the internet through wireless networks.

● ***Counterfeiting***: Counterfeit, remarked, or recycled LSIs are rampant nowadays. It has been estimated that 5% of LSIs in the world market are counterfeit. Producers of LSIs suffer from the costs of detection and protection against counterfeiting as well as the damage to their brand images. Consumers of LSIs suffer from losses in terms of money, quality, health, and safety. For example, fake low-quality remarked operational amplifier LSIs were made and sold to the market, causing huge losses to its genuine maker, Analog Devices, Inc. Counterfeiting also causes severe security concerns. For example, it has been reported that 15% spare LSIs purchased by the U.S. Military from the market are estimated to be counterfeit.

V. Intent of LSI Testing

LSI testing is the technology that are indispensable to mitigate the six major risks of LSIs. The basic concept of LSI testing is illustrated in Fig. 7. In order to conduct LSI testing, test stimuli need to be generated from LSI design data; in addition, (expected) test responses need to be obtained from both test stimuli and LSI design data. Test stimuli are applied to fabricated LSIs through ATE (Automatic Test Equipment) and their actual (test) responses are obtained. ATE then compares (expected) test responses with actual (test) responses. If they fully match, the LSI under test passes the test and is considered a good (defect-free) LSI; if they differ even slightly, the LSI under test fails the test and is considered a bad (defective) LSI.

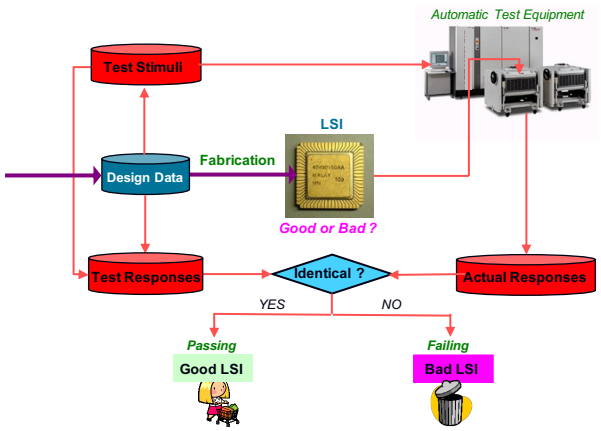


Fig. 7 Concept of LSI Testing

The LSI testing flow in Fig. 7 is mainly targeted at production testing. In practice, LSI testing is a much wider concept spamming from design, manufacturing, and field application. Generally, LSI testing includes all techniques for mitigating the six major risks of LSIs. For this reason, LSI testing is served by its own industry as shown in Fig. 8.

The LSI test industry mainly consists of three sectors, namely test design, test application, and test equipment. The test design sector takes functional design data as its input, add special test-specific circuitry, and generate test stimuli as well as test responses. Functional and test design data are used to create test specifications while test stimuli and test responses form test data. The test application sector generates test programs based on test specifications and test data. It also creates necessary test fixtures, including performance boards, socket boards, and probe cards. The test equipment sector manufactures ATEs, probers and handlers for carrying out LSI testing.

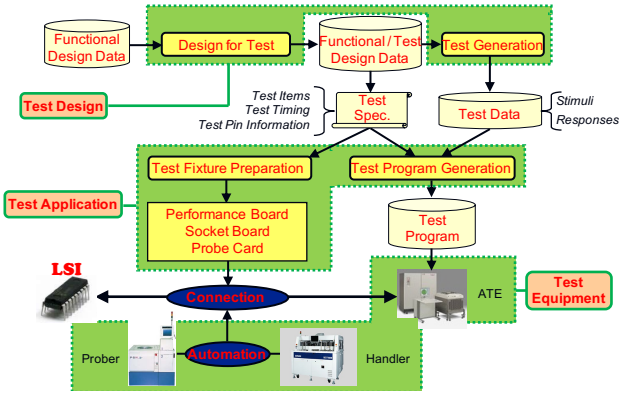
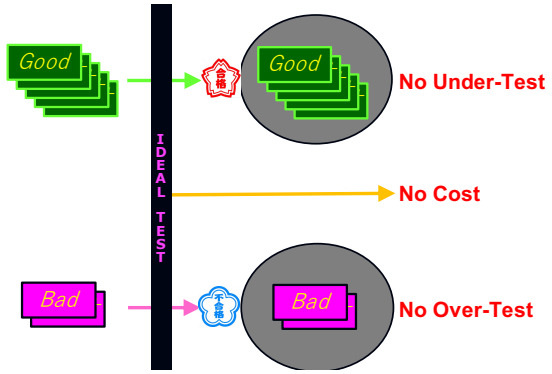


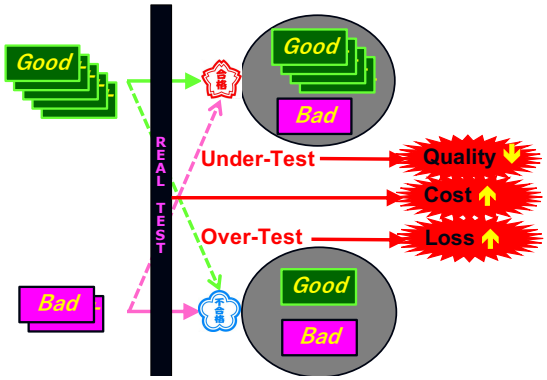
Fig. 8 Sectors of the LSI Test Industry

VI. Impact of LSI Testing

Fig. 9 (a) shows the ideal of LSI testing, which passes all good (defect-free) chips and fails all bad (defective) chips. That is, ideal LSI testing does not incur any under-test, over-test and test costs. However, in reality, LSI testing may pass bad chips, fails good chip, and incurs high test costs, as shown in Fig. 9 (b). That is, under-test and over-test may occur, causing quality degradation and financial losses, respectively. High test costs may even surpass production costs, threatening the viability of the LSI business itself.



(a) The Ideal



(b) The Reality

Fig. 9 LSI Testing: Ideal vs. Reality

The impact of under-test manifests itself as significant in-field risks, especially for such mission-critical applications as satellites, airplanes, trains, nuclear power plants, autonomous cars. The impact of over-test manifests itself as significant revenue losses, especially for such high-end chips as microprocessors for workstations. Furthermore, the growing test costs has become a big burden to the LSI industry. For example, the volume price of a connectivity SoC for IoT applications can be as low as 0.5$, making it very hard to afford its test costs. Therefore, high test quality, low test-induced yield loss, and low test costs are indispensable for the LSI industry.

As illustrated in Fig. 10, LSI testing is an extremely difficult technical field. For example, the size of a defect in a transistor in an advanced LSI chip is $1/10^7$ of the chip size. Detecting for such a defect is as difficult as finding a missing kid from a satellite 10,000km away from the earth.

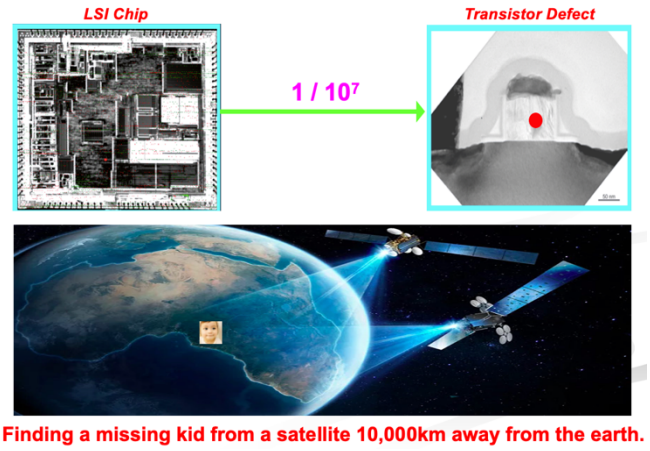


Fig. 10 LSI Testing: A Bottleneck for the LSI Industry

As shown in Fig. 11, LSI testing has become the bottleneck for the LSI industry in recent years due to two trends in terms of technology innovations (from scaling to integrating) and application risks (from low to high). In the past, LSI testing was considered as a cost source. In the earlier years, LSI test technologies were mostly ad-hoc. Later, more advanced LSI test technologies were developed for targeting production defects. High test efficiencies were pursued by making use of similarities in LSI chips but the ROI (Return on Investment) of LSI testing was generally low. In recent years, three major factors have made LSI testing as a core technology for the LSI industry. The first factor is "*diversity*" in terms of processes (FinFET, multi-patterning), architectures (heterogenous processing elements, new memories), and packing (3D, in-memory computing). The second factor is "*test for everything*" as LSI testing is now needed for debug, diagnosis, reliability, security, and safety. The third factor is "*high test ROI*" as LSI testing can serve as a unique competitive weapon and a powerful revenue source. In general, it can be observed that LSI testing has conceptionally evolved from TAC (Test as Cost) to TAV (Test as Value). Furthermore, test engineers, with broad technical skills, a good sense of balance, and good people skills, are now in high demand.

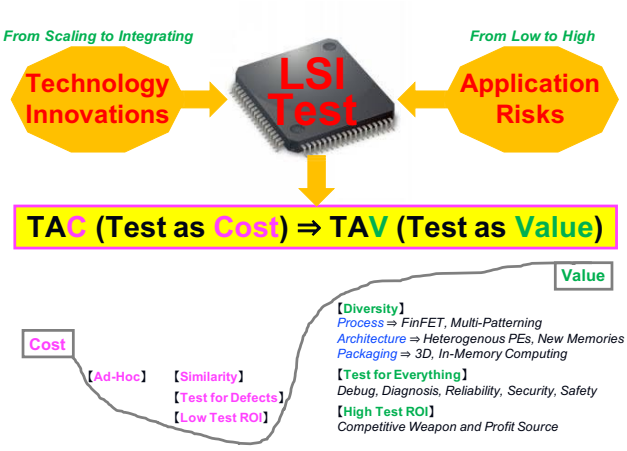


Fig. 11 LSI Testing: A Bottleneck for the LSI Industry

VII. Conclusions

This paper first provided a general review of the LSI industry and pointed out the six major risks faced by LSIs. It then introduced LST testing and highlighted its importance to a successful LSI industry. It is expected this paper will draw the attention of more students and young researchers to LSI testing, an exciting core technology to the LSI industry.

Acknowledgements

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