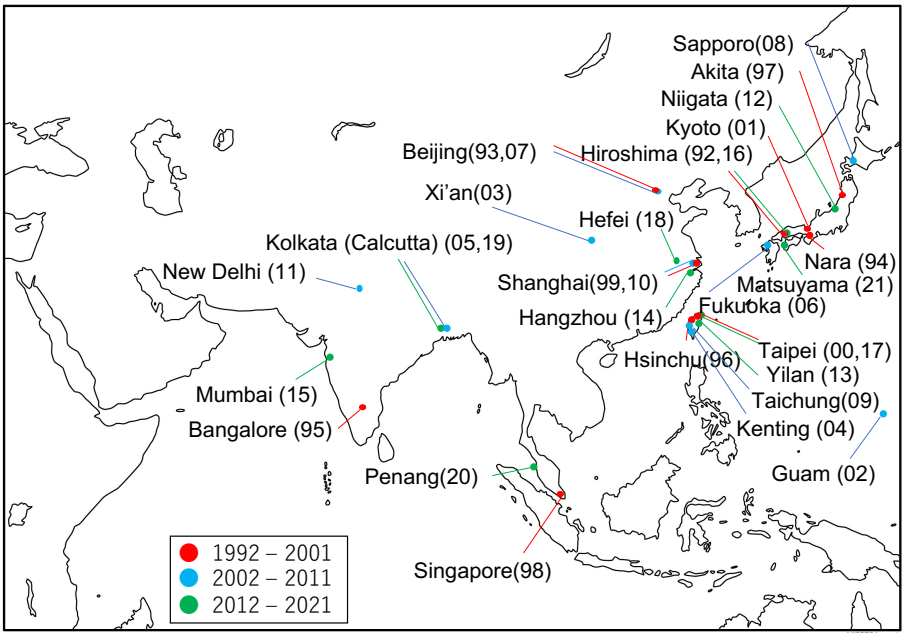
30th Anniversary Compendium of Papers from Asian Test Symposium



Venues of Asian Test Symposium (1992 –2021)

The Asian Test Symposium (ATS) provides an international forum for engineers and researchers from all countries of the world, especially from Asia, to present and discuss various aspects of device, board and system testing with design, manufacturing and field considerations in mind. ATS has been annually held for 30 years at 25 cities (Five cities hosted ATS twice). During these years, ATS has been provided the opportunity to deeply discuss test technology and enhance networking in the research and geographical regions. ATS will continuously play this role in the future.

ATS has published the compendiums of papers twice to commemorate its 10th and 20th anniversaries. This is the third compendiums of papers for our 30th anniversary, that includes five or six best papers from each year of ATS in 2012 – 2021. The compendiums reflect not only the history of ATS but also the transition of research of test technology.

ATS 2012, Niigata, Japan, Novenber 20–23, 2012
Program Chair: Hiroshi Takahashi

Diagnosis of Cell Internal Defects with Multi-Cycle Test Patterns
Xiaoxin Fan, Manish Sharma, Wu-Tung Cheng, Sudhakar Reddy
DOI: 10.1109/ATS.2012.62

SAT-Based Automatic Rectification and Debugging of Combinational Circuits with LUT Insertions
Satoshi Jo, Takeshi Matsumoto, Masahiro Fujita
DOI: 10.1109/ATS.2012.55

TSV Stress-Aware ATPG for 3D Stacked ICs (Best Paper Award)
Sergej Deutsch, Krishnendu Chakrabarty, Shreepad Panth, Sung Kyu Lim
DOI: 10.1109/ATS.2012.61

Scan Test Power Simulation on GPGPUs
Stefan Holst, Eric Schneider, Hans-Joachim Wunderlich
DOI: 10.1109/ATS.2012.23

On-Chip Detection of Process Shift and Process Spread for Silicon Debugging and Model-Hardware Correlation
Islam Mahfuzul, Hidetoshi Onodera
DOI: 10.1109/ATS.2012.66

ATS 2013, Yilan, Taiwan, November 18-21, 2013
Program Chair: J.-L. Huang

Path Constraint Solving Based Test Generation for Hard-to-Reach States
Yanhong Zhou, Tiancheng Wang, Tao Lv, Huawei Li, Xiaowei Li
DOI: 10.1109/ATS.2013.52

Analog Sensor Based Testing of Phase-Locked Loop Dynamic Performance Parameters
Sen-Wen Hsiao, Xian Wang, Abhijit Chatterjee
DOI: 10.1109/ATS.2013.19

MIRID: Mixed-Mode IR-Drop Induced Delay Simulator
Jie Jiang, Mariane Comte, Marina Aparicio, Florence Azais, M. Renovell, Ilia Polian
DOI: 10.1109/ATS.2013.41

Securing Access to Reconfigurable Scan Networks
Rafal Baranowski, Michael Kochte, Hans-Joachim Wunderlich
DOI: 10.1109/ATS.2013.61

On the Generation of Compact Deterministic Test Sets for BIST Ready Designs
Amit Kumar, Janusz Rajski, Sudhakar Reddy, Thomas Rinderknecht
DOI: 10.1109/ATS.2013.45

ATS 2014, Hangzhou, China, November 16-19, 2014
Program Chairs: Yinhe Han, Qiang Xu

Leveraging Emerging Technology for Hardware Security – Case Study on Silicon Nanowire FETs and Graphene SymFETs
Yu Bi, Pierre-Emmanuel Gaillardon, X. Sharon Hu, Michael Niemier, Jiann-Shiun Yuan, Yier Jin
DOI: 10.1109/ATS.2014.69

Design, Verification, and Application of IEEE 1687
Farrokh Ghani Zadegan, Erik Larsson, Artur Jutman, Sergei Devadze, René Krenz-Baath
DOI: 10.1109/ATS.2014.28

Diagnosing Cell Internal Defects Using Analog Simulation-Based Fault Models
Huaxing Tang, Brady Benware, Michael Reese, Joseph Caroselli, Thomas Herrmann, Friedrich Hapke, Robert Tao, Wu-Tung Cheng, Manish Sharma
DOI: 10.1109/ATS.2014.58

A Scalable and Parallel Test Access Strategy for NoC-Based Multicore System
Taewoo Han, Inhyuk Choi, Hyunggoy Oh, Sungho Kang
DOI: 10.1109/ATS.2014.26

Reliability-Driven Pipelined Scan-Like Testing of Digital Microfluidic Biochips
Zipeng Li, Trung Anh Dinh, Tsung-Yi Ho, Krishnendu Chakrabarty
DOI: 10.1109/ATS.2014.22

ATS 2015, Bombay, India, November 22-25, 2015
Program Chair: Adit Singh

Logic/Clock-Path-Aware At-Speed Scan Test Generation for Avoiding False Capture Failures and Reducing Clock Stretch
Koji Asada, Xiaoqing Wen, Stefan Holst, Kohei Miyase, Seiji Kajihara, Michael A. Kochte, Eric Schneider, Hans-Joachim Wunderlich, Jun Qian
DOI: 10.1109/ATS.2015.25

On Improving Transition Test Set Quality to Detect CMOS Transistor Stuck-Open Faults
Xijiang Lin, Wu-Tung Cheng, Janusz Rajski
DOI: 10.1109/ATS.2015.24

A Methodology for Identifying High Timing Variability Paths in Complex Designs
Ankush Srivastava, Virendra Singh, Adit D. Singh, Kewal K Saluja
DOI: 10.1109/ATS.2015.27

At-Speed Testing of Inter-Die Connections of 3D-SICs in the Presence of Shore Logic
Konstantin Shibin, Vivek Chickermane, Brion Keller, Christos Papameletis, Erik Jan Marinissen
DOI: 10.1109/ATS.2015.21

Challenge Engineering and Design of Analog Push Pull Amplifier Based Physically Unclonable Function for Hardware Security
Sabyasachi Deyati, Barry Muldrey, Adit Singh, Abhijit Chatterjee
DOI: 10.1109/ATS.2015.29

TestExpress – New Time-Effective Scan-Based Deterministic Test Paradigm
Jerzy Tyszer, Grzegorz Mrugalski, Janusz Rajski, Jedrzej Solecki And Chen Wang
DOI: 10.1109/ATS.2015.11

ATS 2016, Hiroshima, Japan, November 21-24, 2016
Program Chair: Satoshi Ohtake

On Test Points Enhancing Hardware Security
Elham Moghaddam, Nilanjan Mukherjee, Janusz Rajski, Jerzy Tyszer, Justyna Zawada
DOI: 10.1109/ATS.2016.24

High-Throughput Transistor-Level Fault Simulation on GPUs
Eric Schneider, Hans-Joachim Wunderlich
DOI: 10.1109/ATS.2016.9

Formal Test Point Insertion for Region-Based Low-Capture-Power Compact At-Speed Scan Test
Stephan Eggersgluess, Stefan Holst, Daniel Tille, Kohei Miyase, Xiaoqing Wen
DOI: 10.1109/ATS.2016.41

On Optimal Power-Aware Path Sensitization
Matthias Sauer, Jie Jiang, Sven Reimer, Kohei Miyase, Xiaoqing Wen, Bernd Becker, Ilia Polian
DOI: 10.1109/ATS.2016.63

Efficient Cell-Aware Fault Modeling by Switch-Level Test Generation (Best Paper Award)
Harry Chen, Simon Chen, Po-Yao Chuang, Cheng-Wen Wu
DOI: 10.1109/ATS.2016.33

Functional Diagnosis for Graceful Degradation of NoC Switches
Atefe Dalirsani, Hans-Joachim Wunderlich
DOI: 10.1109/ATS.2016.18

ATS 2017, Taipei, Taiwan, November 27-30, 2017
Program Chairs: Jin-Fu Li

Fault-Aware Page Address Remapping Techniques for Enhancing Yield and Reliability of Flash Memories (Best Paper Award)
Shyue-Kung Lu, Shu-Chi Yu, Masaki Hashizume, Hiroyuki Yotsuyanagi
DOI: 10.1109/ATS.2017.55

Security Implications of Cyberphysical Flow-Based Microfluidic Biochips
Jack Tang, Mohamed Ibrahim, Krishnendu Chakrabarty, Ramesh Karri
DOI: 10.1109/ATS.2017.32

Scan Chain Diagnosis Based on Unsupervised Machine Learning
Yu Huang, Brady Benware, Randy Klingenberg, Huaxing Tang, Jayant Dsouza, Wu-Tung Cheng
DOI: 10.1109/ATS.2017.50

Test and Reliability of Emerging Non-Volatile Memories
Said Hamdioui, Peyman Pouyan, Huawei Li, Ying Wang, Arijit Raychowdhur, Insik Yoon
DOI: 10.1109/ATS.2017.42

Structure-Oriented Test of Reconfigurable Scan Networks
Dominik Ull, Michael Kochte, Hans-Joachim Wunderlich
DOI: 10.1109/ATS.2017.34

Cloud-Based PVT Monitoring System for IoT Devices
Guan-Hao Lian, Shi-Yu Huang, Wei-Yi Chen
DOI: 10.1109/ATS.2017.26

ATS 2018, Hefei, Anhui, China, October 15-18, 2018
Program Chairs: Huawei Li, Xiaoqing Wen, Zhengfeng Huang

Hardware Trojan in FPGA CNN Accelerator
Jing Ye, Yu Hu, Xiaowei Li
DOI: 10.1109/ATS.2018.00024

A Built-in Self-Test Scheme for Detecting Defects in FinFET-Based SRAM Circuit (Best Paper Award)
Meng-Chi Chen, Tsung-Hsuan Wu, Cheng-Wen Wu
DOI: 10.1109/ATS.2018.00015

PUF Based Pay-Per-Device Scheme for IP Protection Of CNN Model
Qingli Guo, Jing Ye; Yue Gong, Yu Hu; Xiaowei Li
DOI: 10.1109/ATS.2018.00032

Extending Aging Monitors for Early Life and Wear-Out Failure Prevention
Chang Liu, Eric Schneider, Matthias Kampmann, Sybille Hellebrand, Hans-Joachim Wunderlich
DOI: 10.1109/ATS.2018.00028

Digital Rights Management for Paper-Based Microfluidic Biochips
Jian-De Li, Sying-Jyan Wang, Katherine Shu-Min Li, Tsung-Yi Ho
DOI: 10.1109/ATS.2018.00042

ATS 2019, Kolkata, India, December 10-13, 2019
Program Chairs: Rubin Parekhji, James Chien-Mo Li

TEA: A Test Generation Algorithm for Designs with Timing Exceptions
Naixing Wang, Chen Wang, Kun-Han Tsai, Wu-Tung Cheng, Xijiang Lin, Mark Kassab, Irith Pomeranz
DOI: 10.1109/ATS47505.2019.000-6

Sanity-Check: Boosting the Reliability of Safety-Critical Deep Neural Network Applications
Elbruz Ozen, Alex Orailoglu
DOI: 10.1109/ATS47505.2019.000-8

Deep Learning Based Test Compression Analyzer
Cheng-Hung Wu, Yu Huang, Kuen-Jong Lee, Wu-Tung Cheng, Gaurav Veda, Sudhakar Reddy, Chun-Cheng Hu, Chong-Siao Ye
DOI: 10.1109/ATS47505.2019.000-9

A Structured Approach for Rapid Identification of Fault-Sensitive Nets in Analog Circuits
Sayandeep Sanyal, Amit Patra, Pallab Dasgupta, Mayukh Bhattacharya
DOI: 10.1109/ATS47505.2019.00025

Hierarchical State Space Checks for Errors in Sensors, Actuators and Control of Nonlinear Systems: Diagnosis and Compensation
Md Momtaz, Abhijit Chatterjee
DOI: 10.1109/ATS47505.2019.00026

ATS 2020, Penang, Malaysia (online), November 22–25, 2020
Program Chairs: Chia Yee Ooi, Erik Larsson

Unexpected Error Explosion in NAND Flash Memory: Observations and Prediction Scheme (Best Paper Award)
Yuqian Pan, Haichun Zhang, Mingyang Gong, Zhenglin Liu
DOI: 10.1109/ATS49688.2020.9301575

Fault and Soft Error Tolerant Delay-Locked Loop
Jun-Yu Yang, Shi-Yu Huang
DOI: 10.1109/ATS49688.2020.9301553

NodeRank: Observation-Point Insertion for Fault Localization in Monolithic 3D ICs
Arjun Chaudhuri, Sanmitra Banerjee, Krishnendu Chakrabarty
DOI: 10.1109/ATS49688.2020.9301589

C-Testing of AI Accelerators
Arjun Chaudhuri, Chunsheng Liu, Xiaoxin Fan, Krishnendu Chakrabarty
DOI: 10.1109/ATS49688.2020.9301581

A Sextuple Cross-Coupled SRAM Cell Protected against Double-Node Upsets
Aibin Yan, Yan Chen, Jun Zhou, Jie Cui, Tianming Ni, Xiaoqing Wen, Patrick Girard
DOI: 10.1109/ATS49688.2020.9301569

ATS 2021, Matsuyama, Ehime, Japan (online), November 22 - 25, 2021
Program Chairs: Yoshinobu Higami

On Modeling CMOS Library Cells for Cell Internal Fault Test Pattern Generation
Xijiang Lin Wu-Tung Cheng, Takeo Kobayashi, Andreas Glowatz
DOI: 10.1109/ATS52891.2021.00030

SeGa: A Trojan Detection Method Combined with Gate Semantics
Yunying Ye, Shan Li, Haihua Shen, Huawei Li, Xiaowei Li
DOI: 10.1109/ATS52891.2021.00020

GPU-Accelerated Timing Simulation of Systolic-Array-Based AI Accelerators
Stefan Holst, Lim Bumun, Xiaoqing Wen
DOI: 10.1109/ATS52891.2021.00034

Detection of Stuck-at and Bridging Fault in Reversible Circuits Using an Augmented Circuit
Mousum Handique, Jantindra Kumar Deka, Santosh Biswas
DOI: 10.1109/ATS52891.2021.00022

Effective SAT-Based Solutions for Generating Functional Sequences Maximizing the Sustained Switching Activity in a Pipelined Processor

Nikolaos Deligiannis, Riccardo Cantoro, Tobias Faller, Tobias Paxian, Bernd Becker, Matteo Sonza Reorda
DOI: 10.1109/ATS52891.2021.00025

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