2016 International Symposium on Dependable Integrated Systems

February 29, 2016
Graduate Seminar Room 7F, General Research Building, Iizuka Campus
Dependable Integrated Systems Research Center, Kyushu Institute of Technology

■ 09:30~09:40 Opening & Introduction to DISC
Xiaoqing Wen, Professor and Director of DISC, Kyushu Institute of Technology, Japan

■ 09:40~10:15 Invited Talk 1

・**Cyber Security & Future Cyberspace: Mission Based Access Control**
Eduard Babulak, Professor, Institute of Technology and Business, Czech Republic

■ 10:15~10:20 Break

■ 10:20~10:55 Invited Talk 2

・**Multi Metric Preferential Algorithm for Partially Re-Configurable Targets**
Amlan Chakrabarti, Associate Professor, A.K. Choudhury School of I.T., University of Calcutta, India

■ 10:55~11:00 Break

■ 11:00~11:35 Invited Talk 3

・**Industrial Approach for Dependability in the Recent Decade**
Nobuyasu Kanekawa, Chief Researcher, Hitachi Research Laboratory, Hitachi Ltd., Japan

■ 11:35~13:00 Lunch

■ 13:00~14:40 DISC Research Presentation I (LSI Design)
Chair: Kohei Miyase, Assistant Professor, DISC, Kyutech, Japan

1. **Low-Power PHY Design for Factory Automation (FA) Wireless LAN System**
A. M. Kurniawati, L. Lanante Jr., Y. Nagao, and H. Ochi
2. **Fast HW/SW Co-Verification Platform for High Throughput Wireless Communication System**
N. Sutisna, R. Hongyo, L. Lanante Jr., Y. Nagao, M. Kurosaki, and H. Ochi
3. **A Study on Design of Segmental Transmission Line Using Improved Quantum Genetic Algorithm**
K.-X. Luo, M. Kurosaki, and H. Ochi
4. **A DC-balanced Bus-invert Coding for Stabilizing the Intermediate Power Level in Stacked-Vdd LSIs**
A. Rahmat, Y. Kohara, N. Kubo, M. Alimudin, and K. Nakamura

■ 14:40~15:00 Break

■ 15:00~16:40 DISC Research Presentation II (LSI Test)
Chair: Leonardo Lanante , Assistant Professor, DISC, Kyutech, Japan

5. **Delay Measurement for Field Test in FPGAs**
Y. Miyake, Y. Sato, and S. Kajihara
6. **An Evaluation of Temperature Voltage Monitor with the TEG chip for Field test**
T. Kato, T. Itonaga, Y. Miyake, Y. Sato, and S. Kajihara
7. **Logic/Clock-Path-Aware At-Speed Scan Test Generation for Avoiding False Capture Failures and Reducing Clock Stretch**
K. Asada, X. Wen, S. Holst, K. Miyase, S. Kajihara, M. A. Kochte, E. Schneider, H.-J. Wunderlich, and and J. Qian
8. **Capture-Safe At-Speed Scan Pattern Generation Concerning IR-Drop Affecting Both Logic Paths and Clock Paths**
F. Li, X. Wen, S. Holst, K. Miyase, S. Kajihara, M. A. Kochte, E. Schneider, and H.-J. Wunderlich

■ 16:40~17:00 Closing
Seiji Kajihara, Vice-Dean of School of Computer Science and Systems Engineering, Kyushu Institute of Technology, Japan

All presentation files are available for download at https://dl.dropboxusercontent.com/u/64915293/DISC-2016_Files.zip