# Power-Aware Testing
# *for*
# Low-Power VLSI Circuits


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# Background

High Performance → **Successful LSI Product** ← Low Power

***Function-Mode***

Call | Cam
Web | Mail

**Low Functional Power**
(*Wide Use of PMS*)

Function → Test

*Growing Power Gap*

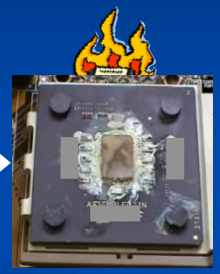
***Test-Mode***

Call | Cam
Web | Mail

**High Test Power**
(*Needs to Handle PMS*)

*Excessive Heat • Timing Failures*

*Higher Test Complexity due to PMS*



**Test Power Related Crisis**
(*Damage / Low Yield / High Cost*)

# Outline

1. Test Power Problems
2. Power Analysis for Power-Aware Test
3. Power Management for Power-Aware Test
4. Future Research Topics

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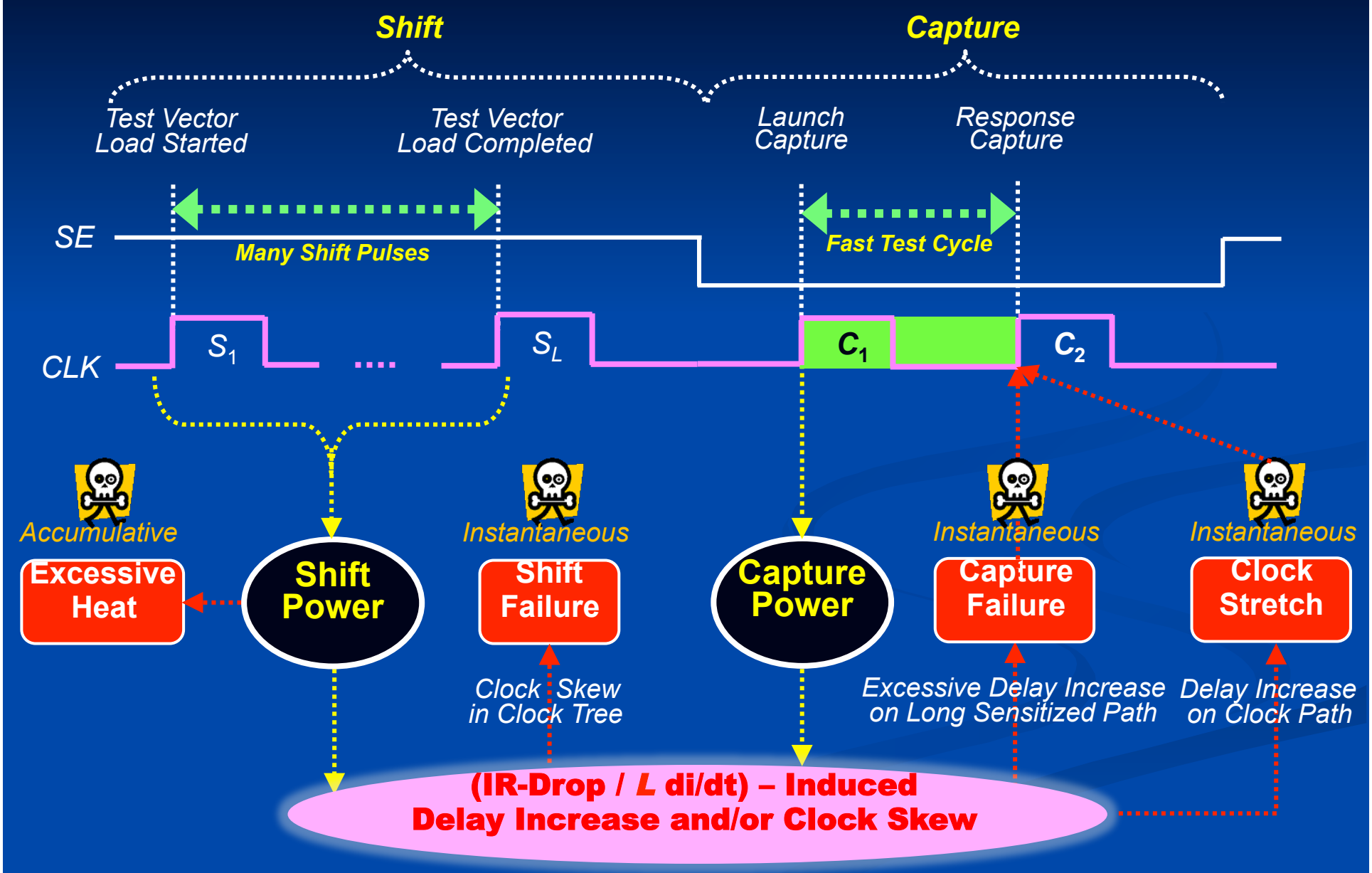
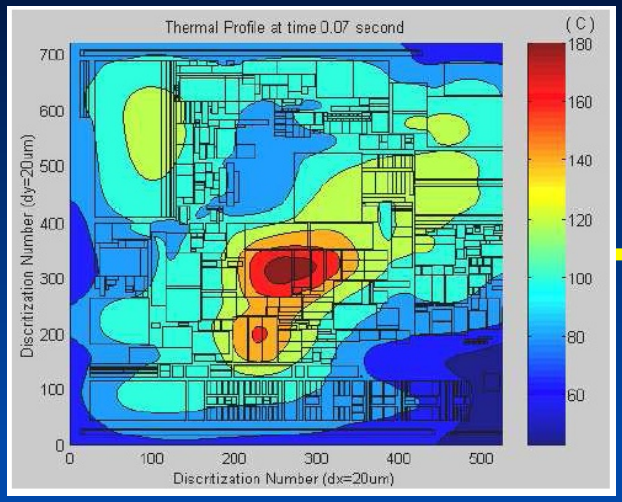
# Impact of Test Power in At-Speed Scan Testing (LOC)

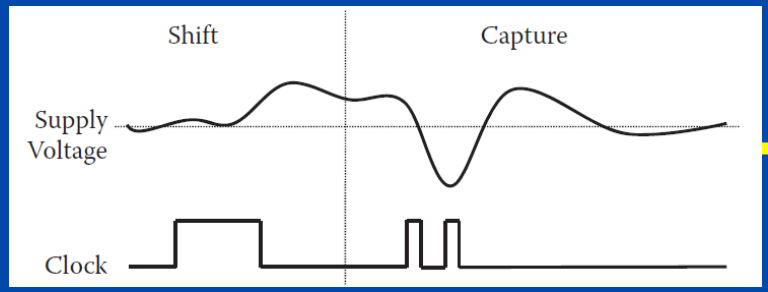


# Test Power Problems: *P1 ~ P4*




**P1**
**Excessive Heat**

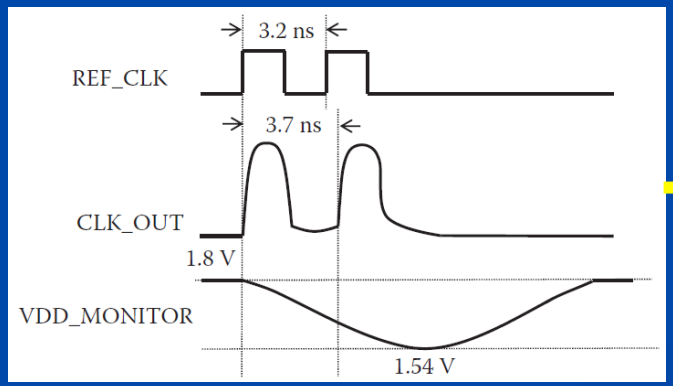
*Chip Damage*
*Reduced Reliability*
*High Test Cost*




**P2**
**Shift Failure**

**P3**
**Captuere Failure**

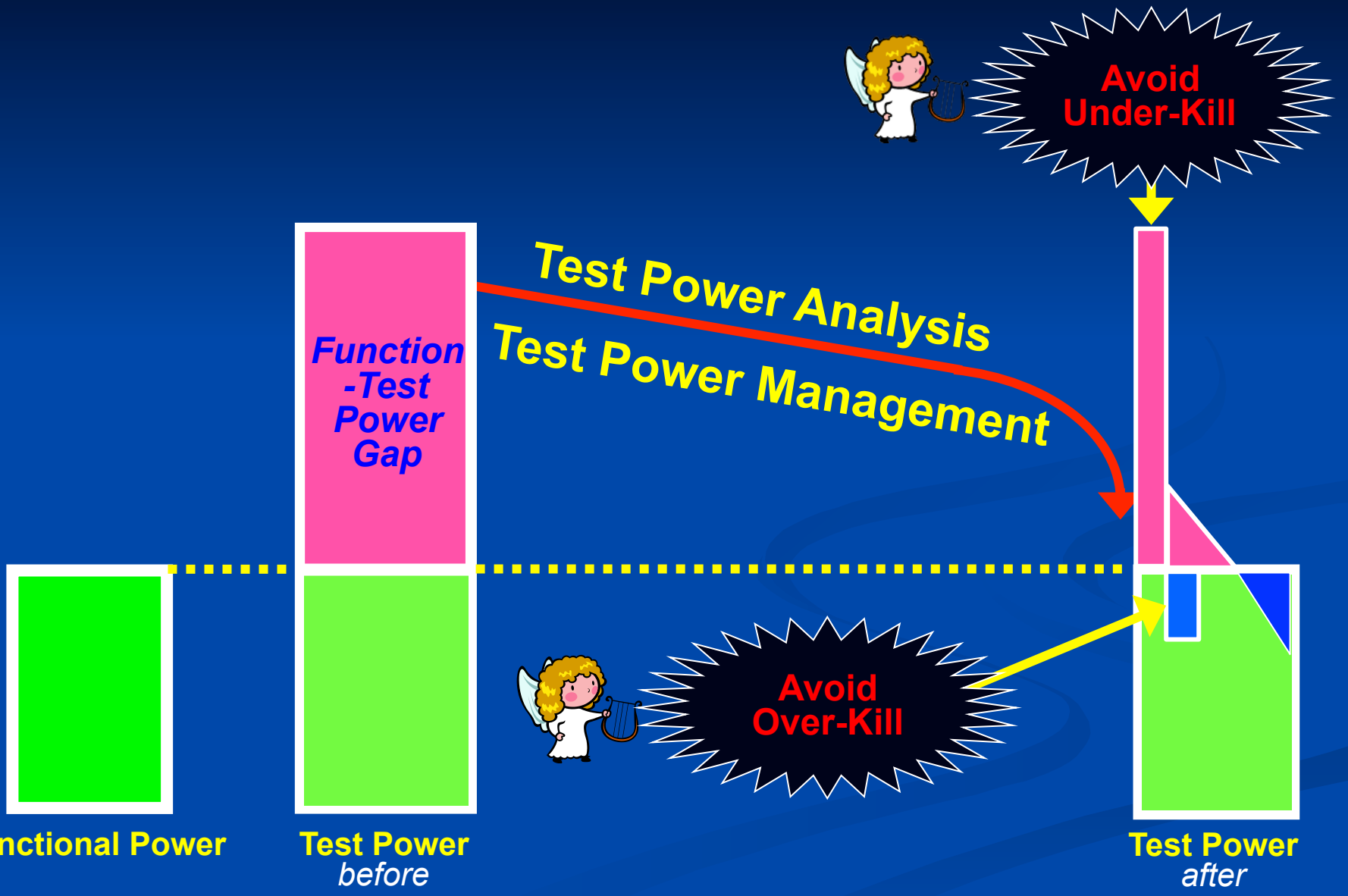
*False-Test-Induced Yield Loss*




**P4**
**Clock Stretch**

*Low Test Quality*
*Low Reliability*

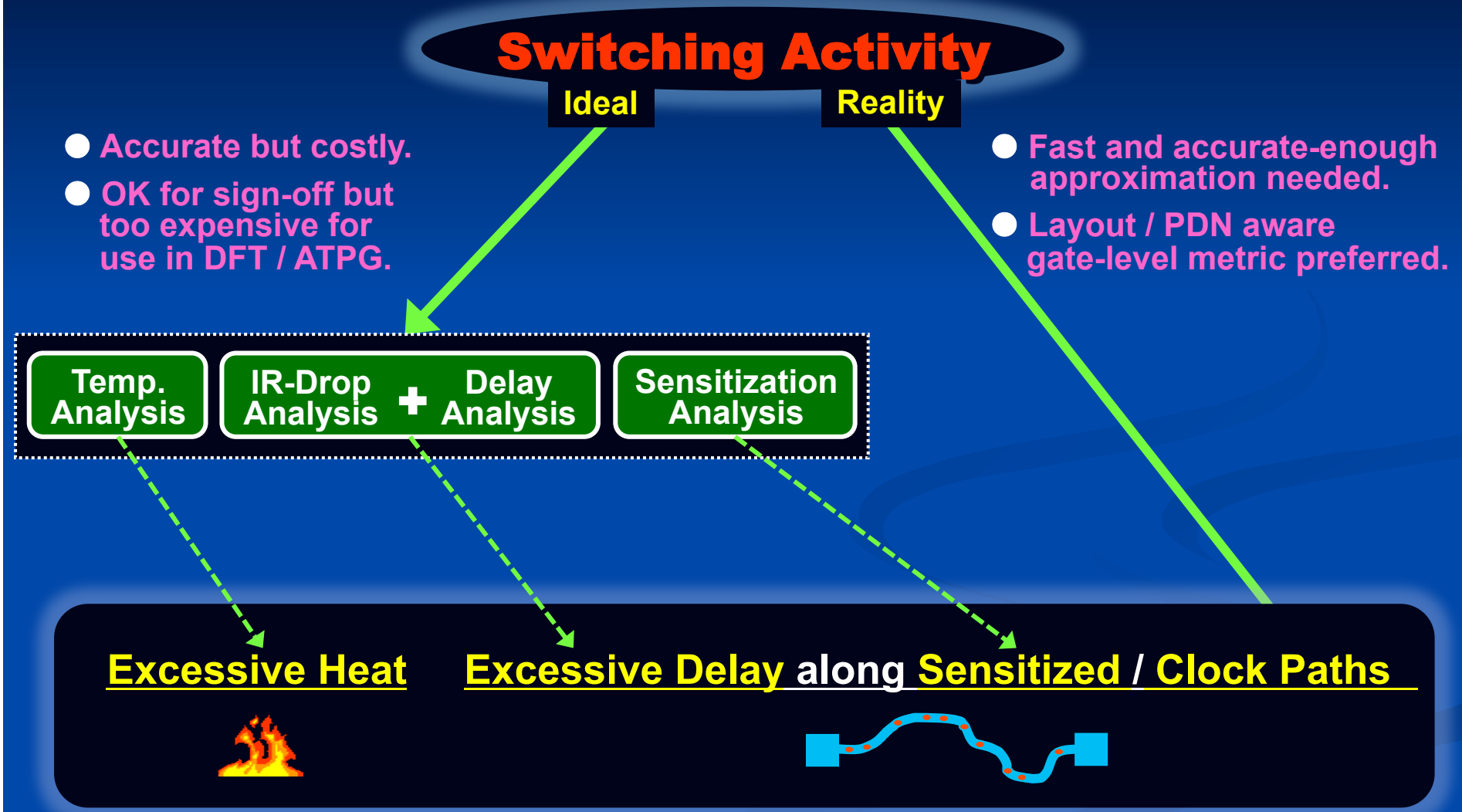
# Power-Aware Test



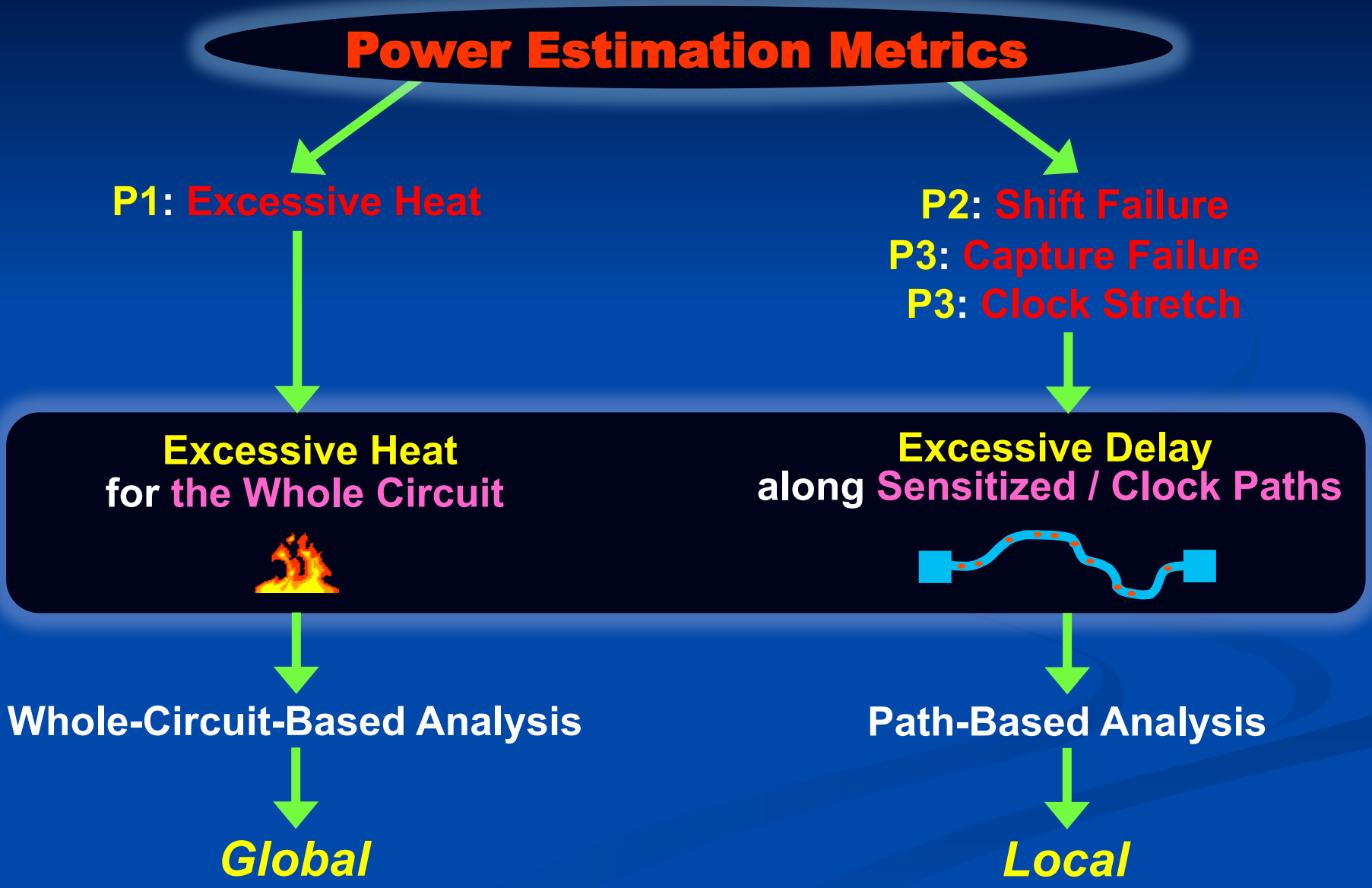
# Outline

1. Test Power Problems
2. **Power Analysis for Power-Aware Test**
3. Power Management for Power-Aware Test
4. Future Research Topics

# Ideal vs. Reality

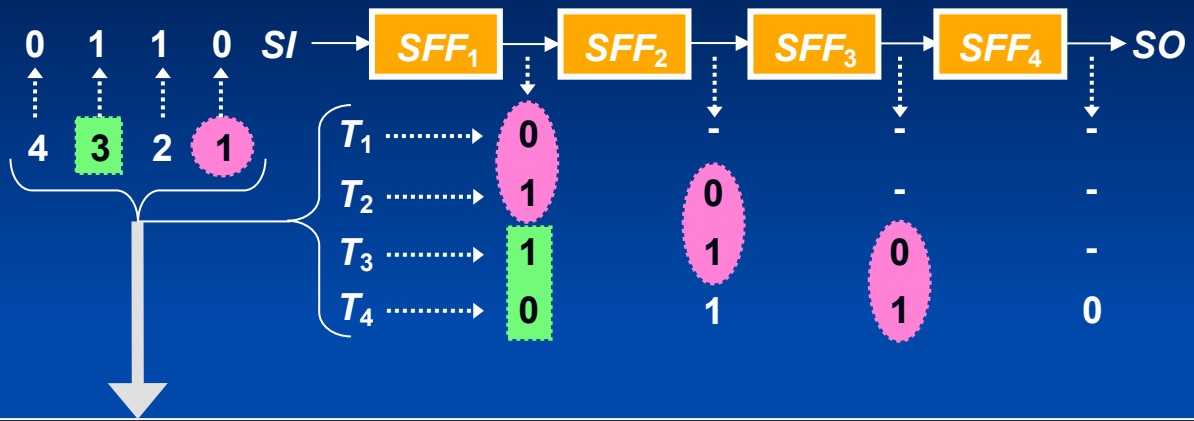


# Power Estimation Metrics



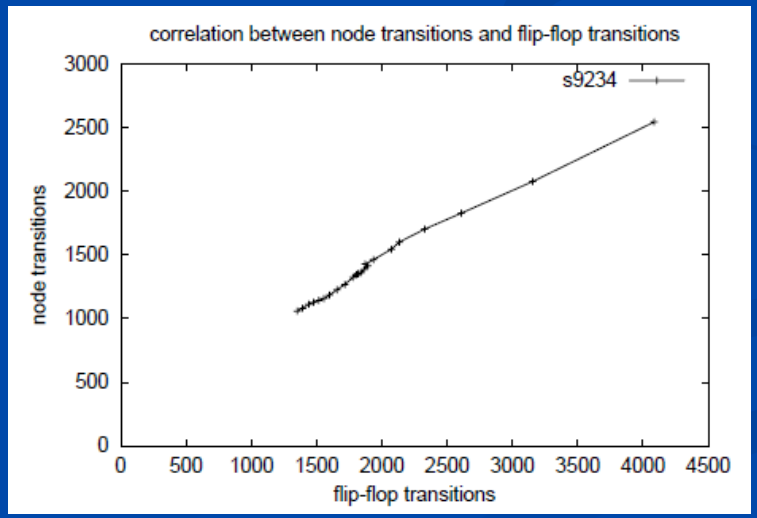
# Global Shift Power Analysis *for Excessive Heat (P1)*

## Estimating Accumulative Impact of Shift Power




$$\textbf{Weighted\_Transitions} = \sum (\text{Scan\_Chain\_Length} - \text{Transition\_Position})$$

*Switching in the CUT* →



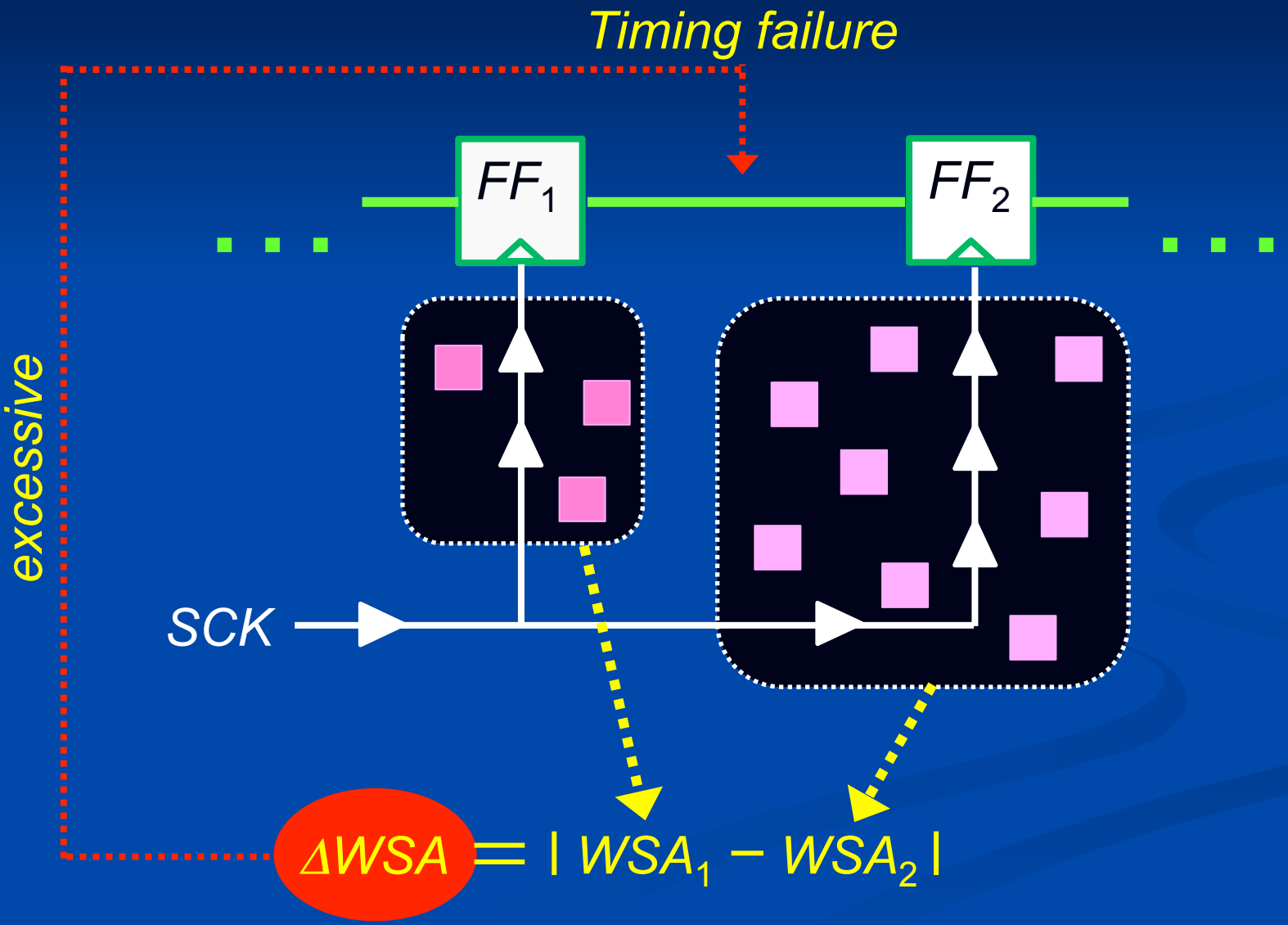

← *Switching at FFs*



(R. Sankaralingam, et al., *Proc. VTS*, pp. 35-40, 2000)

# Local Shift Power Analysis *for Shift Failures (P2)*

## Estimating Inst. Impact of Shift Power on Clock

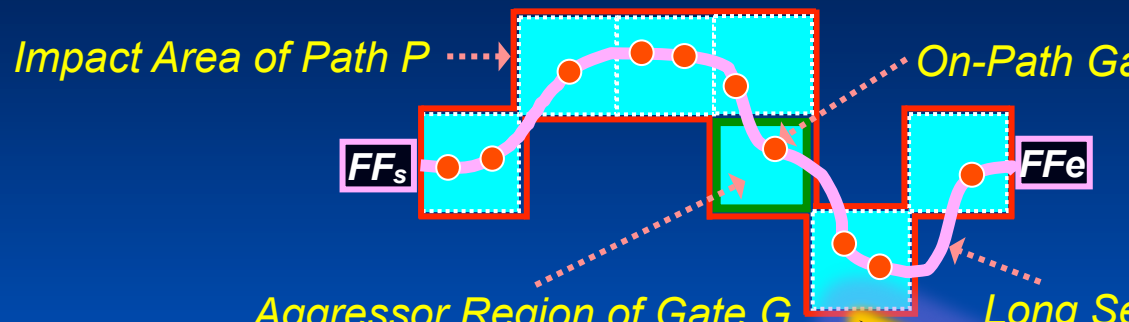


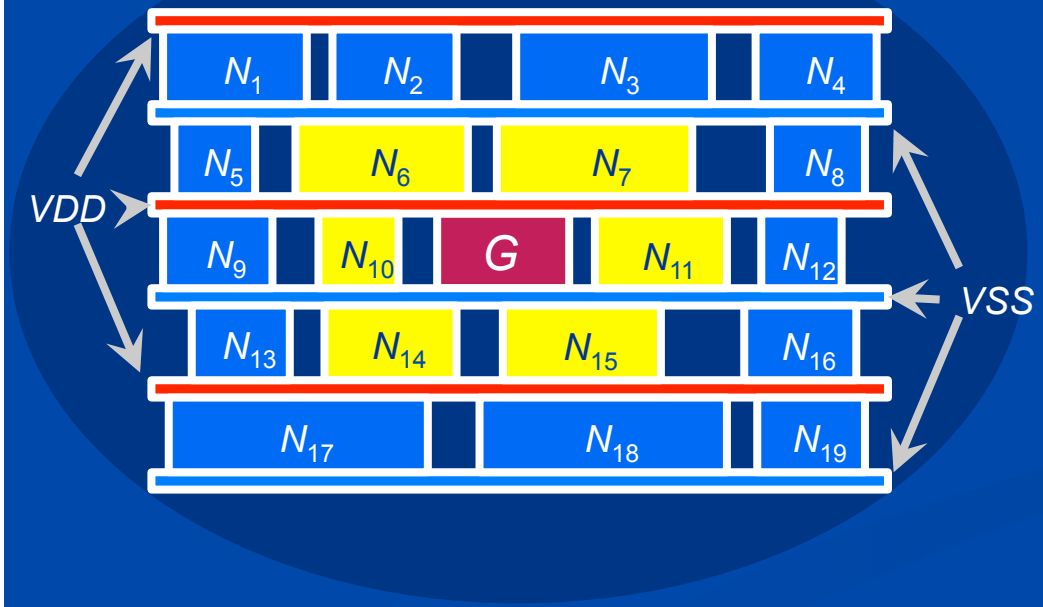



(Y. Yamato, et al., *Proc. ITC*, Paper 12.1, 2011)

# Local Capture Power Analysis *for Capture Failures (P3)*

## Estimating Impact of Capture Power on LSP




WSA of the Impact Area of P

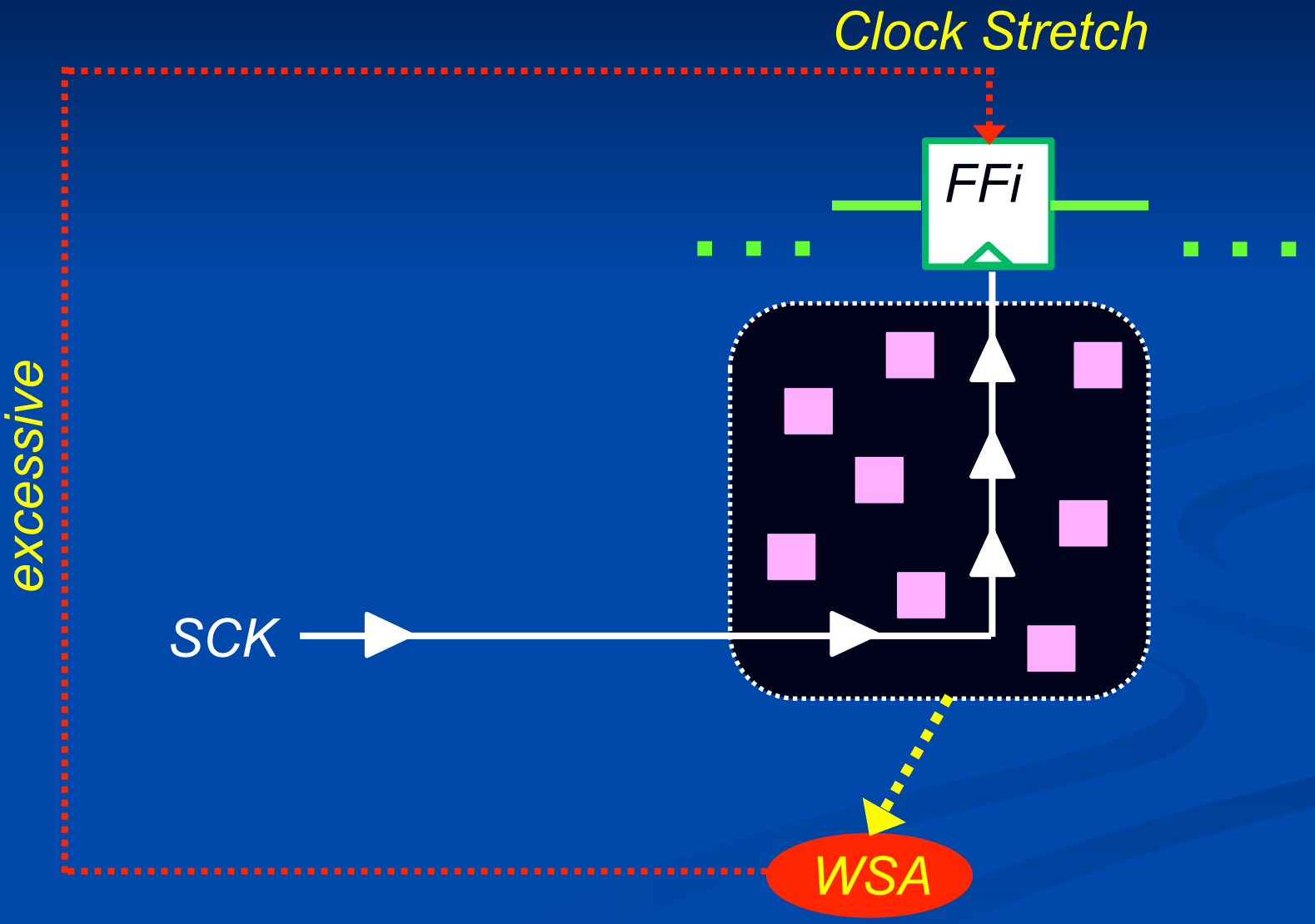
- **Large** → *P is risky*
- **Small** → *P is safe*



(X. Wen, et al., *Proc. VTS*, pp. 166-171, 2011)

# Local Capture Power Analysis *for Clock Stretch (P4)*

## Estimating Impact of Capture Power on Clock



# Outline

1. Test Power Problems
2. Power Analysis for Power-Aware Test
3. **Power Management for Power-Aware Test**
4. Future Research Topics

# Requirements of Power-Aware Test

**Temperature-Safety**

**Shift-Failure-Safety**

**Capture-Failure-Safety**

**Clock-Stretch-Safety**

# ATPG Technique for Capture-Failure-Safety

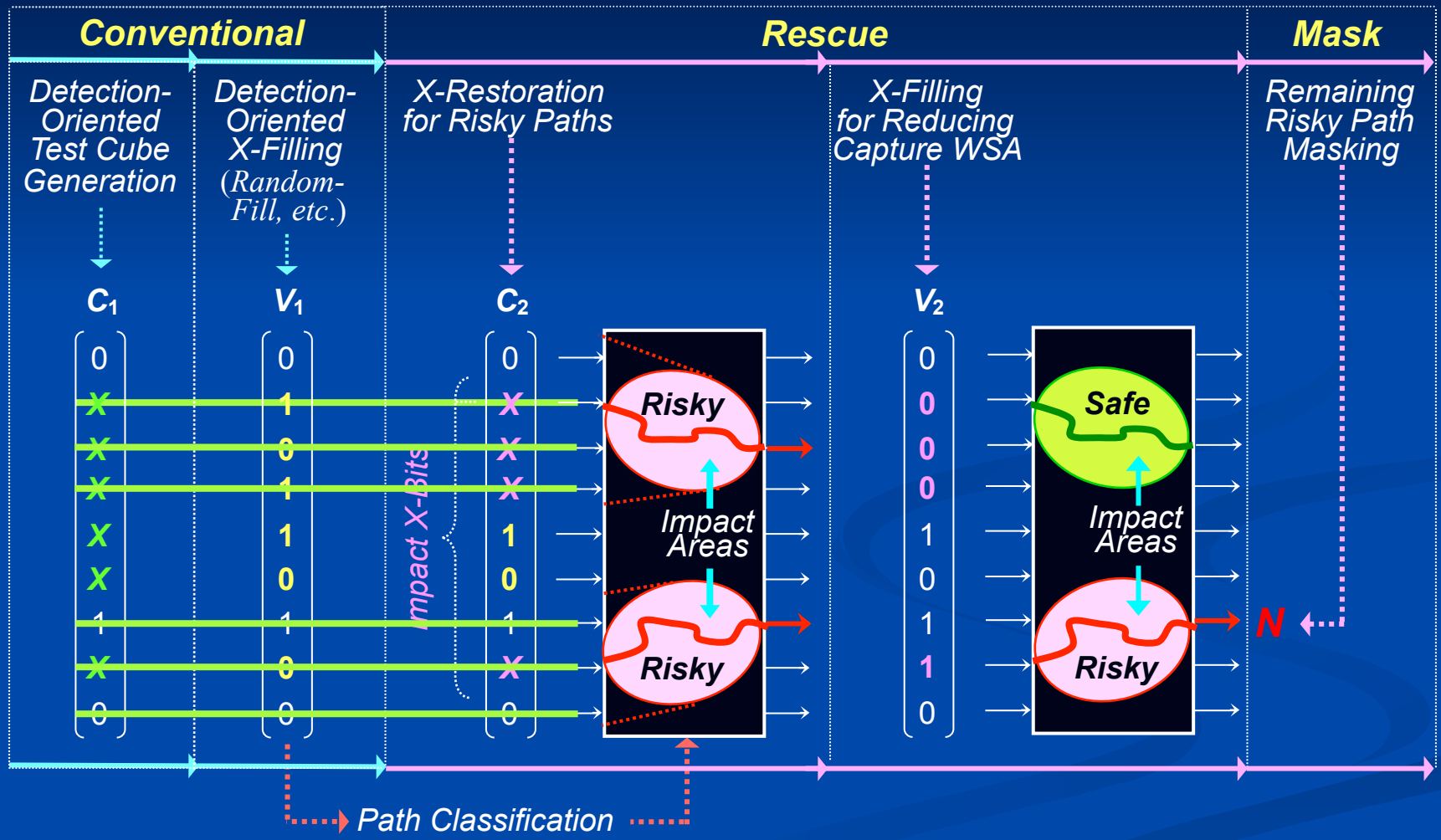
## Capture-Failure-Safety

**Rescue**

**&**

**Mask**

# For Capture-Failure-Safety: *Example*






(X. Wen, et al., *Proc. ITC*, Paper 13.1, 2012)

# For Capture-Failure-Safety: *Results (Commercial ATPG)*

| *Circuit* | *# of Vectors* | *% Risky Vectors* | *FC (%)* | *BCE (%)* | *SDQL* | *CPU (Sec.)* |
|---|---|---|---|---|---|---|
| *b17* | 1,568 | 3.8 | 82.8 | 39.3 | 1358.4 | 491 |
| *b18* | 2,592 | 1.9 | 78.0 | 46.6 | 1292.8 | 1,869 |
| *b19* | 3,776 | 0.2 | 76.0 | 45.6 | 3329.1 | 2,196 |
| *b20* | 1,280 | 2.2 | 80.9 | 43.1 | 282.3 | 264 |
| *b21* | 1,330 | 3.9 | 83.1 | 42.9 | 187.8 | 224 |
| *b22* | 1,444 | 13.0 | 81.4 | 44.2 | 255.7 | 533 |

- *Risky test vectors (i.e., vectors with risky paths) do exist.*
- *Metrics for assessing test quality:*
  - ***FC**: Fault Coverage*
  - ***BCE**: Bridge Coverage Estimate*
  - ***SDQL**: Small Delay Quality Level*



(X. Wen, et al., *Proc. ITC*, Paper 13.1, 2012)

# For Capture-Failure-Safety: *Results (Proposed ATPG)*

| *Circuit* | *Δ# of Vectors (%)* | *% Risky Vectors* | *ΔFC (%)* | *ΔBCE (%)* | *ΔSDQL (%)* | *CPU (Sec.)* |
|---|---|---|---|---|---|---|
| *b17* | 0.20 | 0 | 0.14 | -0.45 | -2.02 | 683 |
| *b18* | 1.45 | 0 | 0.06 | -0.41 | -0.17 | 2,931 |
| *b19* | 0.15 | 0 | 0.03 | -0.07 | -0.65 | 3,229 |
| *b20* | 0.21 | 0 | 0.08 | +1.86 | +0.63 | 532 |
| *b21* | 0.17 | 0 | 0.05 | -1.10 | -0.98 | 394 |
| *b22* | 0.30 | 0 | 0.11 | -0.68 | -2.03 | 1,150 |

- *Capture-failure-safety is guaranteed.*
- *Impact on and test data volume is insignificant.*
- *Impact on test quality (FC, BCE, SDQL) is negligible.*



(X. Wen, et al., *Proc. ITC*, Paper 13.1, 2012)

# ATPG for Capture-Failure-Safety & Clock-Stretch-Safety

**Capture-Failure-Safety**

**Clock-Stretch-Safety**

**Rescue**

**&**

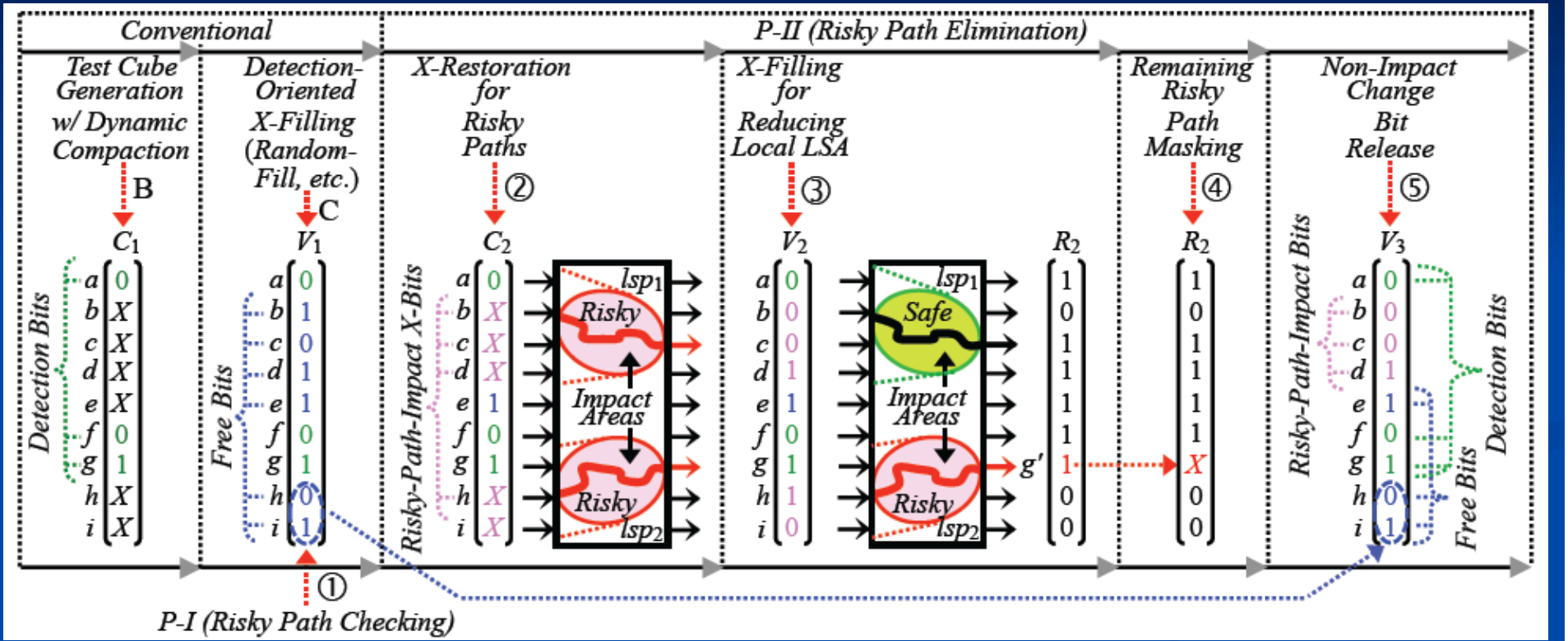
**Mask**

**&**

**Reduction**

# ATPG for Capture-Failure-Safety and Clock-Stretch-Safety

## *Example (1/2)*

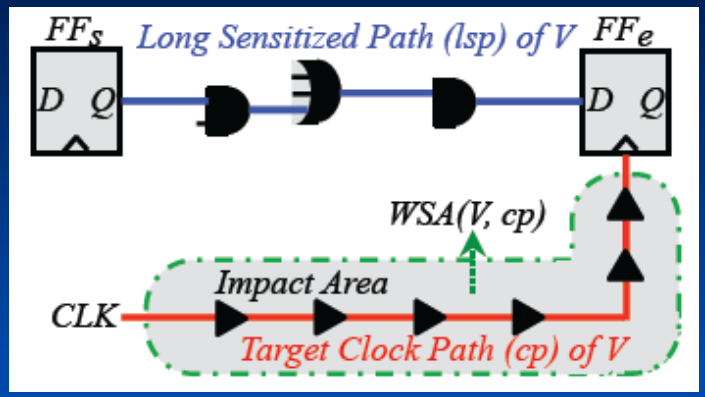


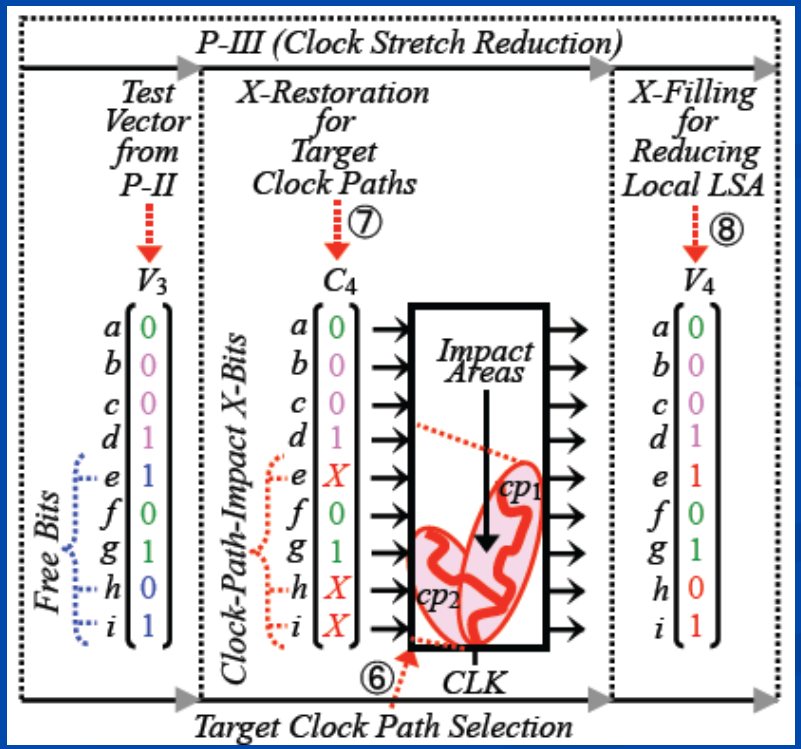



(X. Wen, et al., *Proc. ATS*, 2015)

# ATPG for Capture-Failure-Safety and Clock-Stretch-Safety

## *Example (2/2)*






(X. Wen, et al., *Proc. ATS*, 2015)

# ATPG for Capture-Failure-Safety and Clock-Stretch-Safety

## *Results (Commercial ATPG)*

| Circuit | # of Gates | # of FFs | Max. Path Length | Baseline ATPG (w/o LCP) | | | | | | | ATPG (w/ LCP) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | # of Vectors | FC (%) | BCE (%) | SDQL | # Risky Paths | Ave. WSAcp | CPU (Sec.) | Δ# of Vectors (%) | # Risky Paths |
| *b17* | 32326 | 1415 | 34 | 1175 | 70.1 | 67.2 | 16.3 | 31 | 167 | 674 | 141.2 | 68 |
| *b18* | 114621 | 3320 | 47 | 2428 | 63.6 | 64.8 | 198.9 | 172 | 400 | 5901 | 116.2 | 572 |
| *b19* | 231320 | 6642 | 68 | 3327 | 64.6 | 64.9 | 290.0 | 230 | 425 | 8175 | **182.3** | 809 |
| *b20* | 20226 | 490 | 45 | 1896 | 92.9 | 59.2 | 115.1 | 0 | 420 | 169 | 59.4 | 2 |
| *b21* | 20571 | 490 | 44 | 1870 | 93.2 | 58.9 | 134.7 | 0 | 573 | 139 | 55.5 | 4 |
| *b22* | 29951 | 735 | 50 | 2303 | 93.7 | 63.8 | 139.4 | 83 | 644 | 483 | 39.3 | 120 |

- *Test data inflation is large.*
- *Risks of capture failures remain even with LCP-ATPG vectors.*



(X. Wen, et al., *Proc. ATS*, 2015)

# ATPG for Capture-Failure-Safety and Clock-Stretch-Safety

## *Results (Proposed ATPG)*

| Circuit | Proposed ATPG | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | P-II | | | P-III | Δ# of Vectors (%) | ΔFC (%) | ΔBCE (%) | ΔSDQL (%) | # Risky Paths (initial) | # Risky Paths (final) | ΔAve. WSAcp (%) | CPU (Sec.) |
| | Ave. % of RPI X-Bits | Ave. Rescue Rate (%) | Ave. % of Masked Res. Bits | Ave. % of CPI X-Bits | | | | | | | | |
| b17 | 32.3 | 0 | 78.9 | 45.6 | 4.7 | 0.1 | 0.1 | -0.9 | 38 | 0 | -8.4 | 982 |
| b18 | 17.9 | 0 | 37.0 | 53.7 | 4.2 | 0.0 | 0.5 | -0.1 | 335 | 0 | -23.8 | 7078 |
| b19 | 32.2 | 15.9 | 15.6 | 22.5 | 3.6 | 0.0 | 0.3 | 0.3 | 149 | 0 | -14.8 | 14079 |
| b20 | N/A | N/A | N/A | 39.5 | 8.3 | 0.0 | 1.2 | -0.1 | 0 | 0 | -15.0 | 271 |
| b21 | N/A | N/A | N/A | 35.8 | 4.9 | 0.0 | 1.2 | -0.5 | 0 | 0 | -0.9 | 149 |
| b22 | 16.1 | 0 | 25.7 | 36.1 | 12.6 | 0.0 | 1.2 | -1.0 | 210 | 0 | -18.5 | 379 |
| Ave. | 24.6 | 4.0 | 39.3 | 38.8 | 6.4 | 0.0 | 0.8 | -0.4 | 122 | 0 | -13.6 | |

- *Test data inflation is very small.*
- *Impact on test quality (FC, BCE, SDQL) is negligible.*
- *Capture-failure-safety is guaranteed.*
- *Clock stretch is significantly reduced.*



(X. Wen, et al., *Proc. ATS*, 2015)

# Outline

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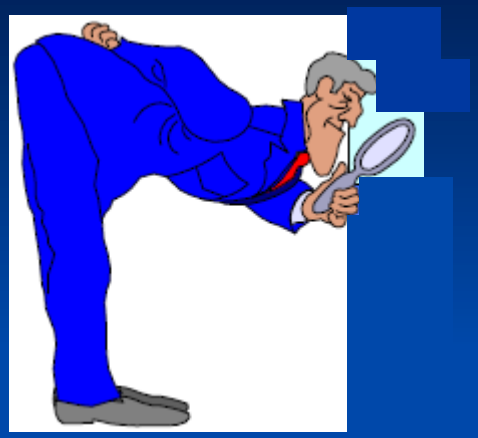
# Topic #1: *GPU-Based Electrical-Level Test Power Analysis*



- ***Which test vector is test-power-risky ?***
- ***What is the problem (P1~P4) ?***
- ***Where is the problem ?***

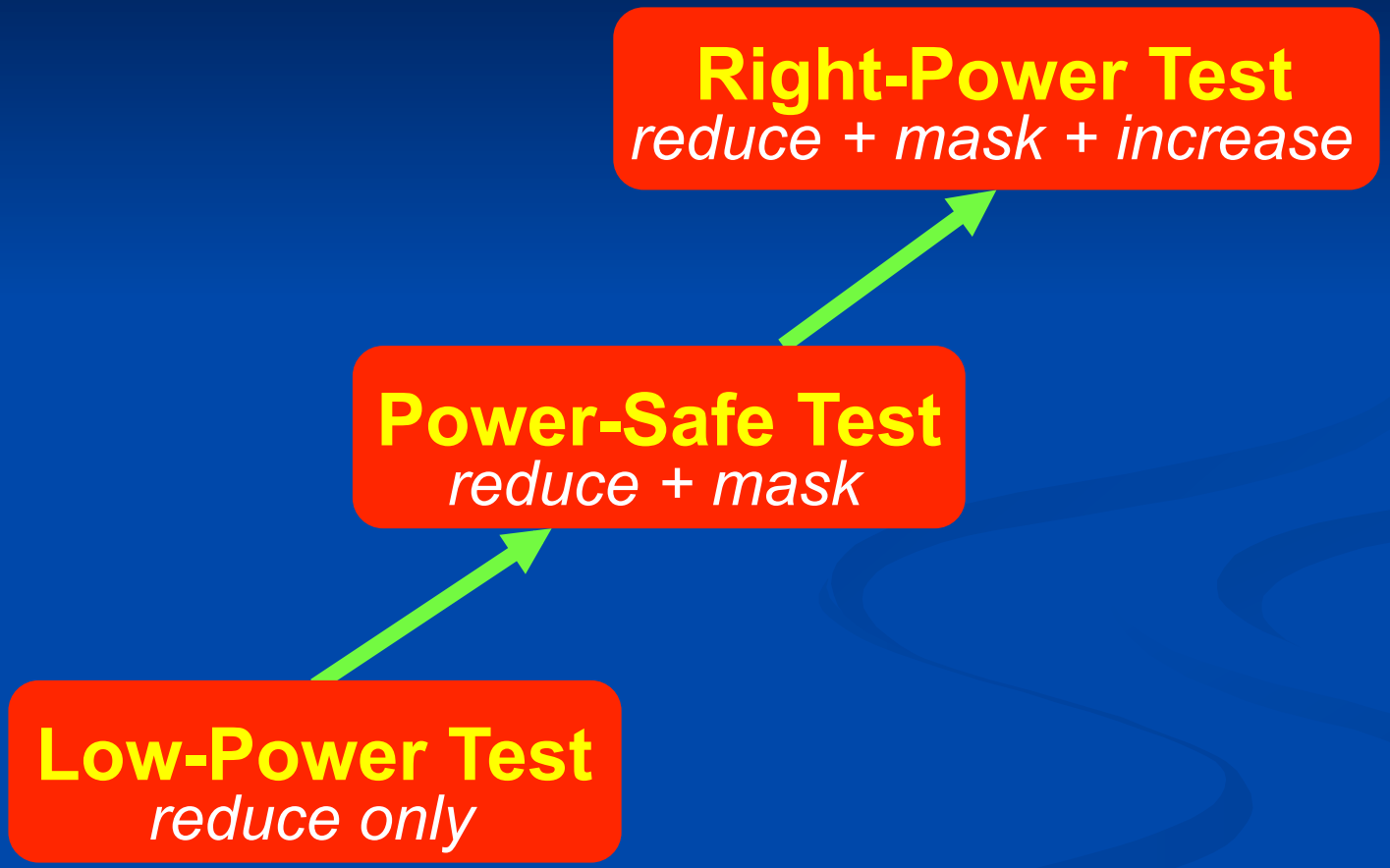
***Full-Timing Electrical-Level Test Power Analysis Needed***

# Topic #2: *Advanced Test Power Management*

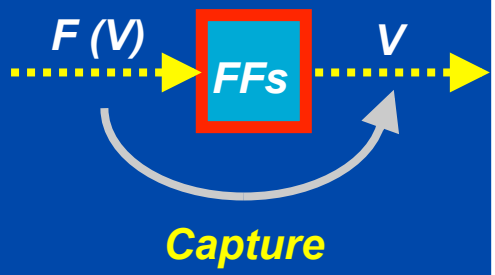
## Test Power Problems

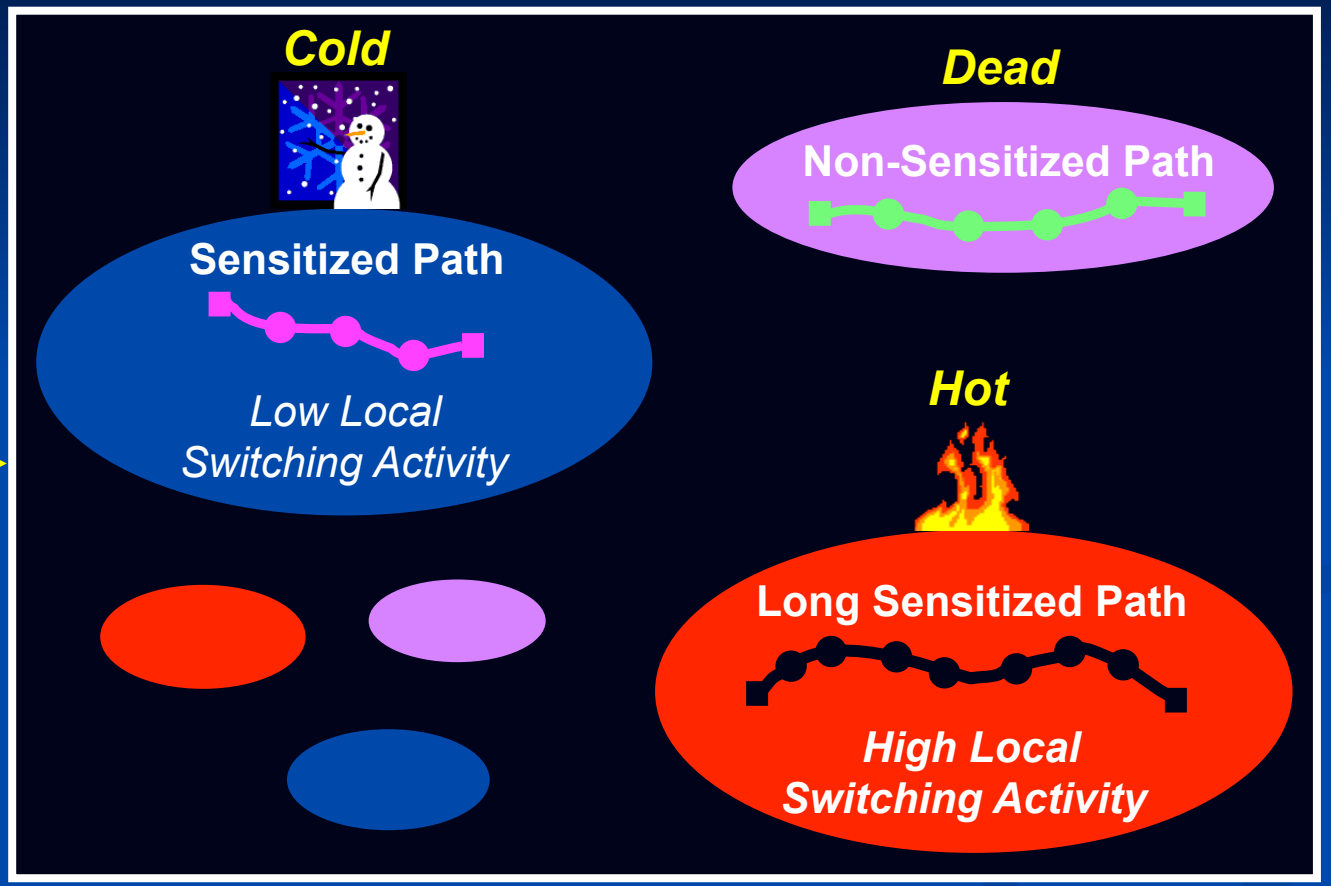
| P1 | P2 | P3 | P4 |
|---|---|---|---|
| Excessive Heat | Shift Failure | Captuere Failure | Clock Stretch |

# Topic #3: *Right-Power Test*



# Right-Capture-Power Test Generation: *Concept*

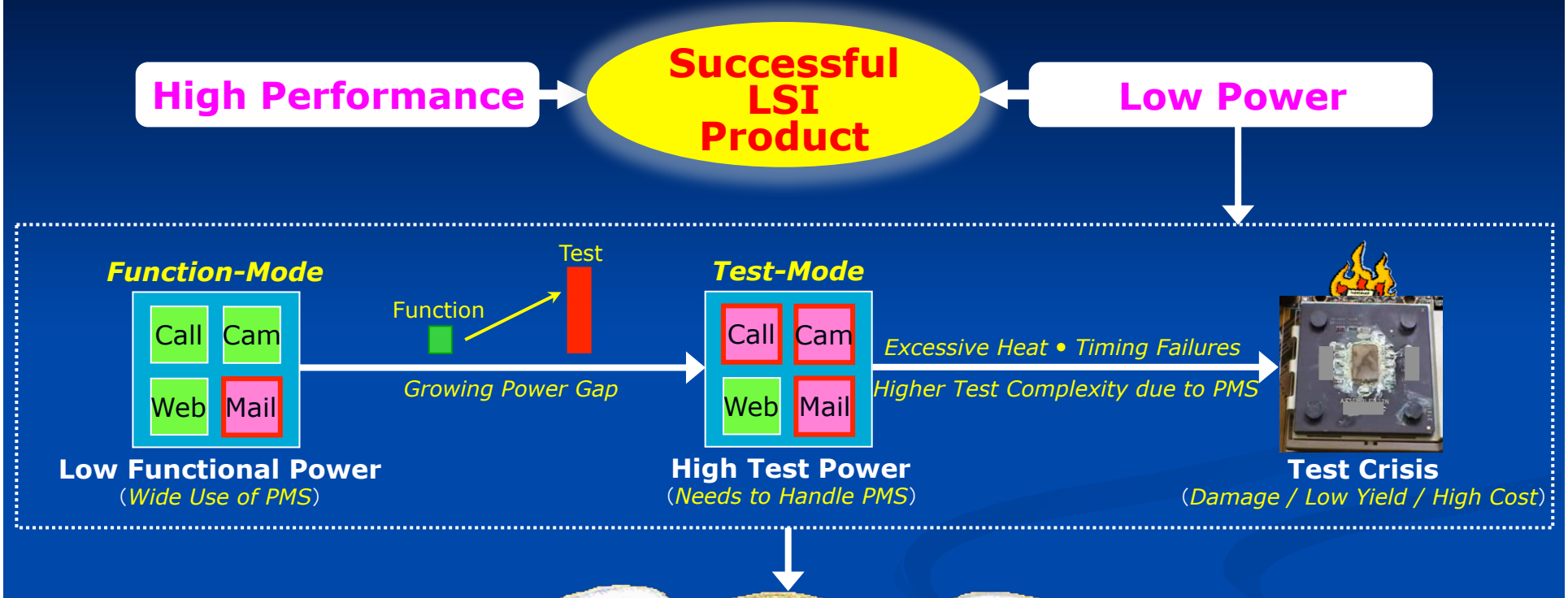



**Pinpoint Capture Power Management**

- No need to consider ***dead areas***.
- ***Hot areas*** must be removed by reducing local switching.
- ***Cold areas*** may be made "*warm*" by increasing local switching.

# Summary




# THANK YOU

*Let us make LSI test **cool**.*