Japan-Taiwan Joint Workshop on Advanced VLSI Testing

May 21th, 2012, Fukuoka, Japan

13:00 ~ 13:05 Opening Xiaoqing Wen (Kyutech)

13:05 ~ 13:35 Keynote Address
"Logic Gating Based Test Power Management"
Jiun-Lang Huang (NTU)

13:35 ~ 14:05
"A Tool Chains to Analyze Soft Error Tolerance for Single Event Transient"
Masayoshi Yoshimura, Taiga Takata, Yusuke Matsunaga (Kyushu U)

14:05 ~ 14:35
"Faster-than At Speed Test for in-Field Reliability"
Tomokazu Yoneda, Keigo Hori and Michiko Inoue (NAIST)

14:35 ~ 14:50 Coffee break

14:50 ~ 15:20
"A Transition Isolation Scan Cell Design for Low Shift and Capture Power"
Yi-Tsung Lin, Jiun-Lang Huang (NTU), Xiaoqing Wen (Kyutech)

15:20 ~ 15:50
"Evaluation of on-Chip Temperature and Voltage Using a Ring-Oscillator-Based Monitor"
Yousuke Miyake, Yasuo Sato, Seiji Kajihara, Kohei Miyase (Kyutech), Yukiya Miura (TMU)

15:50 ~ 16:20
"A Novel Capture-Safety Checking Method for Multi-Clock Designs"
Kohei Miyase (Kyutech), Masao Aso, Ryou Ootsuka (Renesas), Xiaoqing Wen (Kyutech),
Hiroshi Furukawa (Renesas), Yuta Yamato (NAIST), Kazunari Enokimoto, Seiji Kajihara (Kyutech)

16:20 ~ 16:35 Coffee break

16:35 ~ 17:05
"Supply Current Testable DAC of Register-String Type"
Masaki Hashizume, Hiroyuki Yotsuyanagi (U Tokushima), Yukiya Miura(TMU)

17:05 ~ 17:35
"A Test Generation Method for Data Path Circuits Using Functional Time Expansion Models"
Toshinori Hosokawa, Teppei Hayakawa (Nihon U), Masayoshi Yoshimura (Kyushu U)

17:35 ~ 17:40 Coffee break

17:40 ~ 19:30 Free discussion about LSI Testing