令和２年１０月１日

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九州工業大学
ディペンダブル集積システム研究センター（DISC）

特別講演のご案内

日時: 令和２年１０月３０日（金） １０：３０～１２：００

形式: Zoom を利用したオンライン講演
https://kyutech-ac-jp.zoom.us/j/99573435422?pwd=VFBkaldHTzAxOWx2ektDbDR0cmhxdz09
Meeting ID: 995 7343 5422
Passcode: 890594

講師: Prof. Liyang Lai (Shantou University, China)

題目: **GPU-based Hybrid Parallel Logic Simulation for Scan Patterns**

GPGPU, general-purpose computing on graphics processing units, has been witnessed growing from a niche to a mainstream computing paradigm in the last decade. It is widely deployed in machine learning, artificial intelligence, and many scientific applications. In this article, we study gate-level logic simulation for scan test patterns, one of the key algorithmic components for test generation, fault grading and design rule check. We are exploring if GPGPU can deliver scalable performance speedup as promised by its massive parallelism. We discuss the limitations of the state of art work. With GPUs' architectural features in mind, a novel algorithm of hybrid race-tolerant parallel logic simulation is proposed to unleash its immense power of parallelization. Its unique integration of oblivious simulation and event-driven simulation leads to a scalable realization of parallel logic simulation for scan patterns. For the first time in the literature, it is demonstrated that a modest GPU can handle an industrial design of over twenty million gates with excellent performance scalability.

Liyang Lai received his B.S. degree in the department of computer science from Peking University, M.S. from Institute of Microelectronics of Chinese Academy of Sciences, and Ph.D. from the University of Illinois at Urbana-Champaign. From 2005 to 2013, he worked in Silicon Test Division at Mentor Graphics and later became a Consulting Staff at Calypto Design Systems. Since 2015 he has been an associated professor in the Department of Electrical Engineering at Shantou University, China. His research interests include VLSI design and test, fault tolerant computing, and high level synthesis. He is a member of the IEEE and recipient of Best Paper Award of 2006 International Test Conference.

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