令和元年５月３０日

九州工業大学

ディペンダブル集積システム研究センター（DISC）

特別講演のご案内

日時: 令和元年６月17日（月） １３：００～１４：３０

会場: 九州工業大学 飯塚キャンパス（福岡県飯塚市川津680-4）
Global Communication Lounge（福利施設１F）

講師: **Ashutosh Kumar Singh 教授**（National Institute of Technology, **Kurukshetra, India**）

講演題目: **Testing of Reversible Circuits**

Reversible logic circuits are theoretically proven for providing nearly energy-free computation. It has wide applications in the field of quantum computing, optical computing, and nanotechnology. The true functioning of these circuits is another issue where testing plays an important role to meet the destiny of future electronics, since reversible circuits perform bijective functions in which a unique output state is obtained from every input state. Therefore, the operations are fully controllable and observable. This property is utilized by the researchers to incorporate testability in these circuits. Several testing methodologies have been proposed in the literature for the recognition of various types of fault models by means of single-/multiple-bit faults detection, as any fault occurrence results in the change of single/multiple values of bits to the output wires of the circuit. These methodologies are well-categorized in three main classifications, explicitly, designing using proposed gates designing using modification of standard circuits or gates, and designing with inbuilt testability features. It is noticed that the parity preservation and generation principle is preferred in most of the methods due to bijective property of reversible logic circuits. The researchers either proposed novel gates or modified the original circuit in order to produce the necessary information for testing by means of parity bits. The combination of $R1$ and $R2$ online testable gates to form testable logic block TB and the combination of OTG with Feynman gate to form are the major innovations seen in the case of designing using proposed gates methodology. The conversion of a standard gate to form testable reversible cell (TRC) extended Toffoli gate-based conversion and gates cascading approach is found prominent in the case of designing using modification methodology. The process of designing leads to a large increment in operating costs in terms of number of inputs, gate count, quantum cost (QC), and garbage output (GO). In the above context, we present a method of converting an arbitrary circuit into corresponding testable design. In the proposed work, parity preserving gates are first converted into their respective modified testable cells (MTCs), which are used to design an arbitrary circuit. The resulting circuit is cascaded with a derived identity gate to incorporate test and locate functionality which provides full coverage of several types of fault models under single-bit fault detection. Multiple controlled Fredkin (MCF)-gates-based circuits are taken for design and implementation process.

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講師プロフィール

Dr. Ashutosh Kumar Singh is an esteemed researcher and academician in the domain of Electrical and Computer engineering. Currently, he is working as a Professor and Head; Department of Computer Applications; National Institute of Technology; Kurukshetra, India. He has more than 18 years research, teaching and administrative experience in various University systems of the India, UK, Australia and Malaysia. Dr. Singh obtained his Ph. D. degree in Electronics Engineering from Indian Institute of Technology-BHU, India; Post Doc from Department of Computer Science, University of Bristol, United Kingdom and Charted Engineer from United Kingdom.

His research area includes Verification, Synthesis, Design and Testing of Digital Circuits, Predictive Data Analytics, Data Security in Cloud, Web Technology. He has published more than 160 research papers till now in peer-reviewed journals, conferences and news magazines and in these areas. He has also co-authored seven books including “Web Spam Detection Application using Neural Network”, “Digital Systems Fundamentals” and “Computer System Organization & Architecture”. He has worked as principal investigator/investigator for six sponsored research projects and was a key member on a project from EPSRC (United Kingdom) entitled “Logic Verification and Synthesis in New Framework”.

Dr. Singh has visited several countries including Australia, United Kingdom, South Korea, China, Thailand, Indonesia, Japan and USA for collaborative research work, invited talks and to present his research work. He had been entitled for 13 awards such as Merit Awards-2003 (Institute of Engineers), Best Poster Presenter-99 in 86th Indian Science Congress held in Chennai, INDIA, Best Paper Presenter of NSC’99 INDIA and Bintulu Development Authority Best Postgraduate Research Paper Award for 2010, 2011, 2012.

He has served as an Editorial Board Member of International Journal of Networks and Mobile Technologies, International journal of Digital Content Technology and its Applications. Also he has shared his experience as a Guest Editor for Pertanika Journal of Science and Technology, Chairman of CUTSE International Conference 2011, Conference Chair of series of International Conference on Smart Computing and Communication (ICSCC), and as editorial board member of UNITAR e-journal. He is involved in reviewing process in different journals and conferences of repute including IEEE transaction of computer, IET, IEEE conference on ITC, ADCOM etc.